<table>
<thead>
<tr>
<th>Education</th>
<th>Ethics</th>
</tr>
</thead>
<tbody>
<tr>
<td>In GOD’s own land, a fusion of scholastic students, innovative &amp; motivated researchers &amp; teachers and fast moving visionary leaders.</td>
<td>Steeping Stone and Sky reaching ladder to success</td>
</tr>
</tbody>
</table>

**National Institute of Technology, Arunachal Pradesh**  
(Established by Ministry of Human Resource Development, Govt. Of India)

**Course Structure & Syllabus for M-Tech in**  
Electronics Design & Manufacturing

**Research**  
PO- Yupia, Dist. – Papum Pare, Arunachal Pradesh, Pin – 791 112  
Ph No : 0360-2284801/2001582  
Fax No : 0360-2284972  
Email – nitarunachal@gmail.com

**Service to Society**
To achieve the target of being a global leader in the field of Technical Education, there is some sort of time bound urgency to work quickly, massively and strongly, in respect of National Institute of Technology, Arunachal Pradesh being an “Institute of National Importance” (by an Act of Parliament) and being established only in three years back in 2010. I have therefore adopted a ‘B’ formula as stated below to achieve the primary goal of producing world class visionary Engineers and Exceptionally brilliant Researchers and Innovators:

**FORWARD**

In implementing the ‘B’ formula in letter and spirit, the framing of syllabi has been taken as important legitimate parameter. Therefore, extraordinary efforts and dedications were directed for the last one year to frame a syllabi in a framework perhaps not available in the country as of today.

Besides attention on ‘B’ formula institute has given considerable importance to the major faults of current Technical Education while framing the syllabus. The major stumbling blocks in Technical Education today are:

I. The present system is producing “Academic Engineers” rather than “Practical Engineers”.
II. The present system of education makes the students to run after jobs rather than making them competent to create jobs.
III. There is lack of initiative to implement the reality of “Imagination is more important than knowledge”.

Taking due consideration of the findings made above, to my mind a credible syllabi has been framed in the institute in which the major innovations are introduction of:

I. I-Course (Industrial Course) one in each semester at least one, which is targeted to be taught by the Industrial Expert at least up to 50% of its component.
II. Man making and service to society oriented compulsory credit courses of NCC/NSS, values & ethics.
III. Compulsory audit course on Entrepreneurship for all branches.
IV. Many add-on courses those are (non-credit courses) to be offered in vacation to enhance the employability of the students.

V. Many audit courses like French, German, and Chinese to enhance the communication skill in global scale for the students.

VI. Research and imagination building courses such as Research Paper Communication.

VII. Design Course as “Creative Design”.

Further, the syllabi has been framed not to fit in a given structure as we believe structure is for syllabus and syllabus is not for structure. Therefore, as per requirement of the courses, the structure, the credit and the contact hours has been made available in case to case.

The syllabus is also innovative as it includes:

I. In addition to the list of text and reference books, a list of journals and magazines for giving students a flexible of open learning.

II. System of examination in each course as conventional examination, open book examination and online examination.

Each course has been framed with definite objectives and learning outcomes. Syllabus has also identified the courses to be taught either of two models of teaching:

I. J.C.Bose model of teaching where practice is the first theory.

II. S.N.Bose model of teaching where theory is the first practice.

Besides the National Institute of Technology, Arunachal Pradesh has initiated a scheme of simple and best teaching in which for example:

I. Instead of teaching RL, RC and RLC circuit separately, only RLC circuit will be taught and with given conditions on RLC circuits, RL and RC circuits will be derived and left to the students as interest building exercise.

II. Instead of teaching separately High Pass Filter, Band Pass Filter and Low Pass Filter etc.; one circuit will be taught to derive out other circuits, on conditions by the students.

I am firmly confident that the framed syllabus will result in incredible achievements, accelerated growth and pretty emphatic win over any other systems and therefore my students will not run after jobs rather jobs will run after my students.

For the framing of this excellent piece of syllabus, I like to congratulate all members of faculty, Deans and HODs in no other terms but “Sabash!”.

Prof. Dr. C.T. Bhunia
Director, NIT, (A.P.)
In order to achieve the desired goal of excellence and innovations in each and every function of National Institute of Technology, Arunachal Pradesh and to implement ‘B’ Plan in totality, I call upon my distinguished members of Faculty to invest some of their valuable business time in doing Research on Teaching. In this context, I put forward the following general guidelines for teaching practices in the institute:

1) **J.C. Bose Model of Teaching:** As an example, in the Basic Electronics course instead of first teaching the colour codes of the resistors in a theoretical class, teacher may carry few resistors to class and note down on the blackboard the colours of resistors and their values. Thereafter, the teacher may ask the students to device the color code creating enthusiasm among students. Similarly, instead of teaching the characteristics of PN junction diode, teacher may guide the students in a laboratory to draw the characteristics curve, then may advise the students to analyse the behaviour of characteristics. Thereafter, the teacher may teach the theory of PN junction diode.

2) **S.N. Bose Model of Teaching:** This is the conventional model of teaching where theory is first practice but even then I suggest some unique ideas to improve imaginative power and creativity of students in the subject. For example, instead of teaching two algorithms for conversion of decimal to binary, one for integral part and another for fractional part, I call upon the teachers to design a single algorithm for both the purposes for inspiring teaching.

3) I also believe that noble teaching will be simple and in simpler way. Therefore, I call upon the teachers not to teach bandpass filter, low pass filter, high pass filter separately. Teachers may design a single circuit for all filters and put on condition theron can derive separately circuits for separate filters. Similarly, instead of teaching RL, RC and RLC circuits separately, I call upon the teachers to teach only RLC circuit and then putting suitable condition on RLC circuit; RL and RC circuits may be derived and taught.

4) **Last but not the least,** I call upon the teachers to **solve all the problems of all chapters of the main text book prescribed for a subject** in a teaching-learning process – 50% to be solved by teachers (may be of even ones) and 50% may be solved by students (may be odd ones).

I solicit and anticipate full cooperation from all my brilliant pool of young and energetic faculty members to practice the noble and novel teaching procedures explained above without fail. Once **procedures implemented by teachers are documented,** we may proceed to file a patent on **Research in Teaching on behalf of NIT, Arunachal Praesh.**

*Prof. Dr. C.T. Bhunia*
*Director, NIT, (A.P.)*
In recent years, Electronics & Communication Engineering has made unprecedented growth in terms of new technologies, new ideas and principles resulting in extremely high rate of obsolescence of technologies. Researchers, academicians, industries and the society at large have to work in unison to meet the challenges of the rapidly growing discipline. The research organizations and industries that work in this frontier area are in need of highly skilled and scientifically oriented manpower. This manpower can be available only with flexible, adaptive and progressive training programs and a cohesive interaction among the research organizations, academicians and industries. The teaching program contains a proper blend of basic concepts and advances in technology. The faculty has succeeded in keeping a lively atmosphere among the students with innovative teaching techniques. The teaching is closely coupled with the research activities of the department. The ECE Department of NIT Arunachal Pradesh has been consistently working towards this goal. The Department of Electronics & Communication Engineering was established right from inception of the institute in 2010. The department offers a four year degree program in Electronics & Communication Engineering with an annual intake of 30 students & Doctoral program starts in 2013 July session. During these years, this department has diversified its activities in teaching and research. A continuous effort has been put forward towards setting up new laboratories and improves the facilities in the existing laboratories. Following are the laboratories developed with modern infrastructural facilities.

1. Advance Electronic Device & Circuit Lab
2. Electronics Measurement Lab
3. Modern Communication Engineering Lab
4. Embedded System Design Lab
5. Antenna & Propagations Lab
6. Microwave Engineering Lab
7. Digital Signal Processing Lab
8. Simulation Lab

At present research and development activities of department are in the following area:

1. Digital Signal and Image Processing
2. Microwave Patch Antenna
3. VLSI (Very Large Scale Integrated Circuit)
4. Mobile Communication
5. Microcontrollers based systems design.
6. Semiconductor Physics
7. Photovoltaics(PV) devices design

It is our objective to prepare our students to be successful in integrating all the field of engineering and science and to be able to pursue advanced studies in electronics engineering on a competitive global basis. The mission is a culmination of our effort to meet the mission of NIT Arunachal Pradesh, North East region and the nation at large.

1\textsuperscript{st} year the student of ECE department learn about Basic Engineering subject with NCC and one Audit course of French / Korean and German / Chinese which meet Global Standard.2\textsuperscript{nd} and 3\textsuperscript{rd} year student also have Audit course which help to prepare them to face the challenged in Industry. Syllabus also include Industrial Trainings and Project work which help student to fit into industry and research area.
<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
<th>P</th>
<th>T</th>
<th>L</th>
<th>Credit</th>
</tr>
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<tbody>
<tr>
<td>MAS 901</td>
<td>Applied Engineering Mathematics</td>
<td>0</td>
<td>0</td>
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<tr>
<td>ECE 901</td>
<td>Digital System Design</td>
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<td>ECE 902</td>
<td>Advance Semiconductor Devices Architecture</td>
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<td>ECE 903</td>
<td>VLSI Design (Analog and Digital)</td>
<td>2</td>
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<td>ECE 904</td>
<td>Robotics and Industrial Automation in Manufacturing</td>
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<td>HSS 911</td>
<td>Research Methodology</td>
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**SEMESTER – II**

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<td>ECE 905</td>
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<tr>
<td>ECE 906</td>
<td>MEMS &amp; RF based IC Design</td>
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<td>0</td>
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<tr>
<td>ECE 907</td>
<td>DSP Based System Architecture</td>
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<td>ECE 908</td>
<td>Advanced Embedded Systems Design</td>
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<td>ECE 909</td>
<td>Elective Paper-I</td>
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<td>ECE 910</td>
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**SEMESTER – III**

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<td>ECE 911</td>
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<td>ECE 912</td>
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<td>ECE 913</td>
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**SEMESTER – IV**

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<td>ECE 914</td>
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<td><strong>Total</strong></td>
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</tbody>
</table>
Syllabus for M-Tech. (Electronics Design & Manufacturing)

ELECTIVE PAPER – I
(For M-Tech 2nd Semester)

<table>
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<th>Subject</th>
<th>P</th>
<th>T</th>
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<th>Credit</th>
</tr>
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<tbody>
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<td>ECE 915</td>
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<tr>
<td>ECE 916</td>
<td>Design of Semiconductor Memories</td>
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<tr>
<td>ECE 917</td>
<td>Computer Architecture &amp; Parallel Processing</td>
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<td>ECE 918</td>
<td>VLSI Design – II</td>
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<td>ECE 919</td>
<td>Electronic Instrumentation Design</td>
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</table>

Teaching Methodology

M-Tech 1st Semester

<table>
<thead>
<tr>
<th>J.C. Bose Model</th>
<th>S.N. Bose Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subject Code</td>
<td>Name of The Subject</td>
</tr>
<tr>
<td>ECE 901</td>
<td>Digital System Design</td>
</tr>
<tr>
<td>ECE 903</td>
<td>VLSI Design (Analog and Digital)</td>
</tr>
<tr>
<td>ECE 904</td>
<td>Robotics and Industrial Automation in Manufacturing</td>
</tr>
<tr>
<td>MAS 901</td>
<td>Applied Engineering Mathematics</td>
</tr>
</tbody>
</table>
Name of the Module: Applied Engineering Mathematics  
Module Code: MAS 901  
SEMESTER:  
Credit: 3 [P=0, T=0, L=3]  
Module Leader:  
No. of Lectures: 46 Hours

Objectives:  
The course is designed to meet the objectives of:  
1. To gather knowledge on differential equations, simple integrals, special functions.  
2. To work linear partial differential equations, diffusion, wave.

Learning outcomes:  
At the end of this module, students are expected to be able to  
1. Understand higher order differential equations, green functions.  
2. Knowledge about oscillatory integrals, evaluating integral transforms.

Subject Matter:

<table>
<thead>
<tr>
<th>UNIT</th>
<th>COURSE CONTENT</th>
<th>Number of Lectures</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNIT I</td>
<td>First order ordinary Differential Equations, Simple Integrals, Higher order</td>
<td></td>
</tr>
<tr>
<td></td>
<td>differential equations, Special Functions: Bessel and linear ODEs, Connections,</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Numerical and asymptotic, Nonlinear boundary value problems, Boundary Layers.</td>
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<tr>
<td>UNIT II</td>
<td>Linear Partial Differential Equations, Diffusion, wave, Laplace and random walks</td>
<td></td>
</tr>
<tr>
<td></td>
<td>and abstract final project, Green functions.</td>
<td>7</td>
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<tr>
<td>UNIT III</td>
<td>Introduction and overview, Dominant balance and polynomial equations, Dimensions</td>
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</tr>
<tr>
<td></td>
<td>and Dimensional Analysis, Introduction to Numerical Asymptotics, Random</td>
<td></td>
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<tr>
<td></td>
<td>polynomial equations and eigen values.</td>
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<tr>
<td>UNIT IV</td>
<td>Integral transforms and oscillatory integrals, Integral transforms of linear</td>
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</tr>
<tr>
<td></td>
<td>equations, Evaluating integral transforms: Colors of the rainbow, Stationary</td>
<td></td>
</tr>
<tr>
<td></td>
<td>phase, Saddle points.</td>
<td>16</td>
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</tbody>
</table>

Teaching/ Learning/ Practice Pattern:  
Teaching : 40%  
Learning : 10%  
Practice : 50%

Examination Pattern:  
1. Theoretical Examination: Open book / Regular Examination and on line.

Reading List:  
A. Books:  
**Syllabus for M-Tech. (Electronics Design & Manufacturing)**

Name of the Module: Digital System Design  
Module Code: ECE 901  
SEMESTER: 1st  
Credit Value: 4 [P=2, T=0, L=3]  
Module Leader: Alak Majumder  
No. of Lectures: 48 Hours

**Objectives:**
The course is designed to meet the objectives of:
1. Design, testing of Clocked Sequential Circuits.
2. Understanding the importance ROM, PROM, CPLD & Xilinx
3. Gathering knowledge on FPGA & its prototyping.

**Learning outcomes:**
Upon completion of the subjects:
1. To provide a strong background in the basics of Verilog HDL.
2. To impart knowledge about the existing FPGA prototyping/ASIC implementation of Advanced Digital Systems

**Subject Matter:**

<table>
<thead>
<tr>
<th>UNIT</th>
<th>COURSE CONTENT</th>
<th>Number of Lectures</th>
</tr>
</thead>
</table>
| UNIT I   | **Combinational Circuit Design:** Multiplexer & Decoder Based Design of Combinational Circuits; Implementation of Full Adder using Multiplexer; Memory Cells - ROM, PROM, EPROM, Static & Dynamic RAM, Refreshing of Dynamic RAM.  
**Sequential Circuit Design:** Review of flip-flops with excitation table; Clocking of Flip-flops; Setup and Hold Times; Moore Circuit; Mealy Circuit; Sequential Circuit Design Basics; Full Adder using D Flip-flop.  
**Programmable logic Devices:** Advantages of PLDs. Classification of PLDs. Concept of PROM, PAL, PLA, Registered PAL, Configurable PAL, GAL – Architecture and Comparison. CPLD and FPGA architecture. Simulation and testing, Types of FPGAs, Xilinx solutions: Xilinx CPLDs and applications areas, JTAG Development and Debugging Support. | 12                 |
| UNIT II  | **Introduction to state machines:** Classification of State Machines. State Machine Applications. Analysis State Machine, State table, State Diagram, State Equation, State reduction and State assignment. Design of Synchronous State Machine (including Counter) and Asynchronous state machine. Design of Pattern Identifier and Vending Machine.  
**System Design using ASM Chart:** Top-down Design Methodology, ASM Chart, Rules of Drawing ASM Chart, Design of Bus Arbiter and its realization using Mux & D-FF, Implementation of Traffic Light Controller with its hardware realization using Mux, D-FF & ROM, Dice Game with its architecture and ASM Chart.  
**Microprogrammed Design:** Introduction to Microprogrammed Design, ASM Chart for a Microprogrammed Design, Microprogrammed ROM Table, Comparison of the Conventional ROM and the Microprogrammed ROM Approaches, Single Qualifier, Double address Design, Single Qualifier, Single Address (SQSA) System Design, ASM chart for SQSA Microprogrammed Implementation, Microprogrammed Table, Implementation of SQSA System using Microprogrammed ROM, MUX and a Counter, Dice Game using Microprogrammed SQSA System. | 10                 |
UNIT III

Verilog HDL: Modeling of combinational circuits. Top-down approach and bottom-up approach. Levels of Abstraction Realization of Combinational Circuits, Modules and ports, Data flow modelling, Gate level modelling, Behavioural modelling and switch level modelling. Verilog Code for Multiplexers and Demultiplexers, Realization of a Full Adder, Realization of a Magnitude Comparator Design Example, Design of a D Flip Flop, Realization of a Register, Realization of a Counter, Realization of a Non–retriggerable Monoshot, Realization of a Right Shift Register, Realization of a Parallel to Serial Converter, Realization of a Model State Machine, Pattern Sequence Detector as a Design Example

UNIT IV

RTL Coding Guidelines: Introduction Dos and Don’ts for Asynchronous and Synchronous Logic Circuit Design, RTL Coding Style, Separation of Combinational and Sequential Circuits, if - else if – else statements for MUX and Priority Encoder Realizations, Verilog Directives – Case Statements Operators Coding Organization: Introduction to Coding Organization, Design Module – a Model, Complete Code for Combinational and Sequential Circuits, Right Shift Register, Parallel to Serial Converter, Model State Machine, Pattern Sequence Detector Writing a Test Bench: Test bench for simple design – AND gate, Test bench for Combinational Circuits Test bench for Sequential Circuits Design of Memories: On-chip Dual ROM & Dual RAM Design, External RAM Design

List of Practical: -
1. Design and Simulation of Full Adder.
2. Design and Simulation of Magnitude Comparator.
8. Using Verilog coding perform the simulation of a Traffic Light Controller.
10. Using Verilog coding perform the simulation of a Non-retriggerable monoshot.
11. Using Verilog coding perform the simulation of a Serial signed Design.
12. Using Verilog coding perform the simulation of a ROM, RAM & External RAM.

Teaching/Learning/Practice Practice Pattern:
Teaching: 40%
Learning: 10%
Practice: 50%

Examination Pattern:
1. Theoretical Examination: Open book/ Regular examination and on line test.

Reading List:
A. BOOKS:
1. R.P. Jain, “Modern Digital Design”, TMH.
3. Digital Logic and State Machine Design, Comer, OUP
Name of the Module: Advance Semiconductor Devices Architecture
Module Code: ECE 902
SEMESTER: 1st
Credit Value: 3 [P=0, T=0, L=3]
Module Leader: Santanu Maity
No. of Lectures: 45 Hours

Objectives:
The course is design to meet with the objectives of:

1. Imparting theoretical and practical knowledge to the students in the area of Heterostructure.
2. Providing teaching and learning to make students acquainting with advanced semiconductor devices.
3. Injecting the future scope and the research direction in the discipline of HBT & HEMT.

Learning Outcomes:
Upon completion of the subject:

1. Students will be adequately trained to research on HBT & HEMT.
2. Students will be skilled both theoretically and practically to use this subject for the application in wireless communication, optical communication and computers.

Subjects Matter:

<table>
<thead>
<tr>
<th>UNIT</th>
<th>COURSE CONTENT</th>
<th>Number of Lectures</th>
</tr>
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<tbody>
<tr>
<td>UNIT I</td>
<td><strong>Introduction:</strong> Need for high speed devices and circuits, High Speed = Short transit time, Short Review of Quantum theory, Bohr theory of atoms, quantum mechanics’ postulates, Quantum mechanical understanding of a particle in potential wells, Block theorem and Kronig Penney model of periodic potential wells, energy band theory of solids, E-K diagrams, Brillonim zones, idea of Holes and effective mass, Mobility of carriers, intervalley electron transfer or Gunn effect, Ballistic transport, Density of states in energy bonds and carrier statistics, Generation - Recombination process, Diffusion and carrier transport</td>
<td>15</td>
</tr>
</tbody>
</table>
SYLLABUS FOR M-TECH. (ELECTRONICS DESIGN & MANUFACTURING)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>Topic</th>
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<tbody>
<tr>
<td>UNIT II</td>
<td>Introduction to heterostructure devices, Semi-classical Theory, HBT, Quantum theory of Heterostructure and quantum heterostructure devices (Quantum Well, RTD, Superlattice), Scattering processes and scattering assisted tunneling in heterostructure devices and high frequency response of quantum devices (RTD, Infrared Laser).</td>
</tr>
<tr>
<td>UNIT III</td>
<td>Charge Control of the Two-Dimensional Electron Gas in HEMT, High Electric-Field Transport in Semiconductor Devices, Current Voltage Models of the Short-Channel MOSFET, HEMT, SOI and LDMOS, Ultra high-speed transistors: ballistic transistors, vertical FETs, Negative Differential Resistance effects in Semiconductors and NDR devices.</td>
</tr>
</tbody>
</table>

Teaching/Learning/Practice Pattern:

Teaching: 70%
Learning: 30%
Practice: 0%

Examination Pattern:

1. Theoretical Examination: Regular Written Examination

Reading List:

A. BOOKS:

B. MAGAZINES:
1. IEEE magazines on Semiconductor manufacturing.

C. JOURNALS:
1. IEEE transactions on solid states circuits
2. IEEE transactions on VLSI
3. Journal of Circuits, systems and computers, world scientific publisher
4. Applied Physics Letter
5. Journal of Nanoscience and Nanotechnology.
**Syllabus for M-Tech. (Electronics Design & Manufacturing)**

Name of the Module: VLSI Design (Analog and Digital)
Module Code: ECE 903
SEMESTER: 1st
Credit Value: 4 [P=2, T=0, L= 3]
Module Leader: Abir Jyoti Mondal
No. of Lectures: 40 Hours

### Objectives:
The course is designed to meet with the objectives of
1. To understand the basics of MOS in different regions of operation and to understand how to apply proper bias voltages so as to operate as a switch or amplifier.
2. To understand the operations of CAD tools in the design and analysis of MOS circuits.

### Learning Outcomes:
Upon Completion of the topics:
1. Students will be able to bias MOS transistors depending on requirements.
2. Knowledge about operations of MOS circuits.

<table>
<thead>
<tr>
<th>UNIT</th>
<th>COURSE CONTENT</th>
<th>Number of Lectures</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNIT I</td>
<td><strong>Introduction:</strong> Historical Perspective, Classification of CMOS Digital Design, VLSI Design Flow, Design Hierarchy. <strong>Basic MOS Device Physics:</strong> General Considerations, MOS I/V Characteristics, Second Order Effects, MOS Device Models. <strong>MOS Transistor:</strong> The Metal Oxide Semiconductor Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current Voltage Characteristics, MOSFET Scaling and Small Geometry Effects, MOSFET Capacitance. <strong>MOS Inverter:</strong> Introduction, Resistive Load Inverter, Inverters with n-Type MOSFET Loads, CMOS Inverter.</td>
<td>10</td>
</tr>
<tr>
<td>UNIT II</td>
<td><strong>MOS Inverter Switching Characteristics:</strong> Introduction, Delay Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Power Dissipation of CMOS Inverters. <strong>Combinational MOS Logic Circuits:</strong> Introduction, MOS Logic Circuits with Depletion nMOS Loads, CMOS Logic Circuits, CMOS Transmission Gates.</td>
<td>10</td>
</tr>
<tr>
<td>UNIT III</td>
<td><strong>Sequential MOS Logic Circuits:</strong> Introduction, Behavior of Bistable Elements, SR Latch Circuits, Clocked Latch and Flip-Flop Circuits, CMOS D Latch and Edge Triggered Flip Flop. <strong>Analog CMOS Subcircuits:</strong> MOS Switch, Current Sinks and Sources, Current Mirrors, Current and Voltage References. <strong>Single Stage Amplifiers:</strong> Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.</td>
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<tr>
<td>UNIT IV</td>
<td><strong>Differential Amplifiers:</strong> The MOS Differential Pair Small Signal Operation of the MOS Differential Pair, Non Ideal Characteristics of the Differential Amplifier, The Differential Amplifier with Active Load. <strong>Frequency Response of Amplifiers:</strong> General Considerations, Common Source Stage, Source Followers, Common gate Stage, Cascode Stage, Differential Pair.</td>
<td>10</td>
</tr>
</tbody>
</table>
List of practical:

1. Study of Tanner EDA tool and to explore the operations of T Editor and S Editor.
2. N-MOS and P-MOS transistors are taken from library and appropriate voltages is applied at gate and drain terminals to obtain the desired current versus voltage waveforms.
3. A CMOS inverter is designed using n-MOS and p-MOS transistors and an appropriate voltage is applied at the input to verify the inverter operation.
4. NAND and AND gates are designed using MOS transistors and an appropriate input is applied to verify the corresponding logic.
5. NOR and OR gates are designed using MOS transistors and an appropriate input is applied to verify the corresponding logic.
6. XOR and XNOR gates are designed using MOS transistors and an appropriate input is applied to verify the corresponding logic.
7. Half adder and Full adder are designed using MOS transistors and an appropriate input is applied to verify the output expression.
8. Half subtractor and Full subtractor are designed using MOS transistors and an appropriate input is applied to verify the output expression.
9. Common Source, Common Drain and Common Gate amplifiers are designed using MOS and an appropriate voltage is applied at the input to verify their output waveforms.
10. A basic Current Mirror is designed using MOS and its output waveform is obtained to verify the relation $I_{out}=I_{ref}$.
11. A Cascoded Current Mirror is designed using MOS and its out waveform is obtained to verify the minimum overdrive voltage.

Teaching/Learning/Practice Practice Pattern:
Teaching: 40%
Learning: 10%
Practice: 50%

Examination Pattern:
1. Theoretical Examination: Open book/ Regular examination and on line test.

READING LIST:

A. Text Books:
4. Design of Analog CMOS Integrated Circuits by Behzad Razavi, TMH.

B. Reference Books:
C. Magazines:
1. IEEE magazines on Semiconductor manufacturing.
3. IEEE magazines on Consumer electronics.

D. Journals:
3. IEEE transactions on VLSI systems.
4. IEEE proceeding of Computer and Digital techniques.

Name of the Module: Robotics and Industrial Automation in Manufacturing
Module Code: ECE 904
SEMESTER: 1st
Credit Value: 3 [P=2, T=0, L=3]
Module Leader: Sahadev Roy
No. of Lectures: 40 Hours

Objectives:
The course is designed to meet with the objectives of:
1. To understand the basic concepts associated with the design and functioning and applications of Robots.
2. To study about the drives and sensors used in Industry.
3. To learn about analyzing robot kinematics and dynamics.

Learning outcomes:
At the end of this module, students will be able to do
1. Utilization of Robots and automatic system in the industry.
2. Design electronics circuits for automatic manufacturing process.

Subject Matter:

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<tr>
<th>UNIT</th>
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<th>Number of Lectures</th>
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<tbody>
<tr>
<td>1</td>
<td>Fundamentals of robotics and industrial automation: robot – definition – robot</td>
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<td>anatomy – co-ordinate systems, work envelope, types and classification –</td>
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<td>specifications – pitch, yaw, roll, joint notations, speed of motion, pay load –</td>
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<td>robot parts and functions – need for robots–inspection, identification, visual</td>
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<td>serving and navigation. Different applications related to manufacturing.</td>
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<td>Economic analysis of robots – pay back method safety considerations for robot</td>
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<td>operations.</td>
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<td>2</td>
<td>Kinematics and dynamics of robotics: forward kinematics, inverse kinematics</td>
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<td>and differences; forward kinematics and reverse kinematics of manipulators with</td>
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<td>two, three degrees of freedom (in 2 dimensional), four degrees of freedom</td>
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<td>(in 3 dimensional) – deviations and problems. Micro robotics architecture.</td>
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<td>3</td>
<td>Drives &amp; Robot Sensors: pneumatic drives – hydraulic drives – mechanical drives</td>
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<td>– electrical drives – d.c. Servo motors, stepper motor, a.c. Servo motors</td>
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<td>features, applications and comparison of drives end effectors – grippers –</td>
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</table>
mechanical grippers, pneumatic and hydraulic grippers, magnetic grippers, vacuum grippers; two fingered and three fingered grippers; internal grippers and external grippers. Robot sensor like motion, vision, sonar, joint movement etc for planning and industrial automation.


Teaching/Learning/Practice Practice Pattern:
Teaching: 50%
Learning: 30%
Practice: 20%

Examination Pattern:
1. Theoretical Examination: Regular examination

List of practical:
1. Design of Control driver of Robot Design of Control panel for Robot Gripper
2. Controller design of Robot link
3. Design of End effectors of Robot
4. Different type of Gripper Design
5. Design of wheel Robot
6. Study application of different sensor for Industrial Robot
7. Any innovative design practices

Reading List:
A. Books
8. 8051 Microcontroller: Hardware, software and Interfacing 2nd edition, Stewart

B. MAGAZINES
1. International Metal Working News.
2. Industrial Distribution

C. JOURNALS
1. International Journal of Machine Tools and Manufacture
2. Journal of Manufacturing Science and Engineering, Transactions of the ASME
3. Journal of Manufacturing Technology and Research
4. Robotics and Autonomous Systems, Elsevier, Netherlands
**Name of the Module:** Research Methodology  
**Module Code:** HSS 911  
**SEMESTER:**  
**Credit:** 3 [P=0, T=0, L=3]  
**Module Leader:**  
**No. of Lectures:** 36 Hours

**Introduction:**

In the last two decades, emerging theories in qualitative research have drawn attention to the complexities inherent in research. In light of these theories, research can no longer be regarded unproblematic, objective, or value free, where data is neutrally and naturally collected, interpreted and textualized by disinterested researchers. Rather, research methodology has become a problematized and contested terrain depicting a double crisis of representation and legitimation. What is (and why) this double crisis? And what implications might it have for the field of qualitative research and for the researcher working (in) that field? Attempting to answer those questions and the various issues underlying them is the primary objective of this course. We will do this by combining a theoretical and practical approach to the study of qualitative methodology in order to “learn to attend to the politics of what we do and do not do (as researchers)” (Lather, P. 1991: 13) and “to ‘read out’ the epistemologies in our various practices” (Hartsock, 1987: 206). The second objective of the course is to explore both the “hows” or research (providing ample opportunities for you to “practice” them) and, at the same time, examine the underlying assumptions and values of qualitative research practices —your own as well as a variety of other strategies and orientations. The third and overarching objective of this course is to examine not only how one goes about “doing” those aspects of one’s work but also delve into a variety of ethical, epistemological, ontological and (naturally) methodological issues inherent in that “doing.”

**Learning outcomes:**

At the end of this module, students are expected to be able to

1. Increased awareness of ethnographic work, including conceptualizing a study, observations, interviewing, analysis, and textualization.
2. To learn to attend to the politics of what we do and do not do (as researchers).
3. Increase critical thinking skills. Demonstrate this by seriously considering multiple viewpoints and perspectives in class discussions, in-class writing, group work, and the final paper.
4. Apply course material to your own research. Demonstrate this through participation in in-class discussions and activities, and in applying course concepts to class assignments.
5. Become active in the process of seeking, analyzing, and synthesizing information.

**Subject Matter:**

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<tr>
<td>UNIT I</td>
<td><strong>Five reading responses/reflective journal entries:</strong> You are required to write a set of five short (3-5 pages) reading responses to a group of readings that will be used/shared in class. With the exception of the Becker book it is up to you to chose the set of readings that you will respond to. These on-going short assignments may include either (a) a response to a, several, or all the readings assigned for class; (b) a commentary on readings for the previous class (following our class discussion) or (c) a response to reflection on an of the class interactions/discussions, etc. about issues relating to course topics. The focus of a Reading Response (which should go beyond summary to include commentary and questions you are left with having engaged the</td>
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</table>
reading(s) can be directed either toward a particular reading assigned for that day’s class or to the readings as a whole—comparing them and possibly relating them to other readings, etc. Journal entries should be a critical reflection on a class discussion or interaction or on one (or a combination of several) of the course readings following our discussion in a previous class. Journal entries could relate to your own academic area of interest and/or (or as they pertain) to what you find to be significant issues addressed by the readings and/or during our in-class discussions—in a way, deconstructing, deepening, or extending them. Responses are to be handed in at the beginning a class.

**UNIT II**

**Interview Assignment:** For this assignment you will select a person (or a group of people) and conduct an interview with them. Your paper should provide: (a) a brief description of the person/people you interviewed, why you interviewed them, and what you hope to achieve through this interview (what you hoped to learn); (b) an interview protocol; (c) a transcript of the interview; (d) an analysis of the interview. The analysis should include two dimensions: 1) what you learned about the topic you were inquiring about through this interview, and 2) what you learned methodologically from this interview. That is, what you learned as a researcher about interviewing from this experience and how might you use what you learned in your future research.

**UNIT III**

**Critiquing a dissertation’s methodology:** (not simply its methods but its methodology). For this assignment, you should select a dissertation (there are various of those in the library) and, using what we have learned in the course, provide a critique of its methodology. By critique I do not merely criticize (this is what is bad with this dissertation) but rather a way to explore—conduct a critical conversation with—the politics of knowledge production in that dissertation: what is the dissertation about? How did the researcher go about producing and making claims to knowledge? What methods did the researcher use? Do you believe those methods were conducive to answer the study’s particular questions and make its particular claims to knowledge and knowing? If so, how? If not, why? To what degree do you believe the methods used in this study matched/enhanced/contradicted the epistemological understandings underlying the topic being studied (in other words, did the study produce a methodology or merely a set of methods)? What do you believe are some of the methodological strengths of this study (and why do you believe that?)? What do you believe are some of the methodological weaknesses of this study (and why do you believe that?)? What did you learn from this critique about conducting qualitative research? How might this knowledge direct you in thinking about your own study? What are some of the notes absences and silences in this study? On what is this study’s methodology silent? Why? With what consequences? How, if at all, does this study deal with the ethical issues and those pertaining to power?

**UNIT IV**

**Final paper:** The purpose of this assignment is to “consolidate” your learning in/from this course. The intent is for you to use this assignment to begin writing (or to consolidate) your research proposal. Your research proposal should include the following: 1) an explanation of the “problem” to be studied; 2) your research questions; 3) a review of the literature that contextualizes the “problem” and identifies gaps in the literature your study hopes to fill in; 4) the ontological, epistemological, and methodological lenses and frames you are bringing to your research; 5) explanation of your choice of location, participants, etc. and the methods (strategies) to be applied in your study (those ought to correlate with what you provided in #4.

Also: gaining access, your role as researcher, how are you going to deal with ethical
Teaching/ Learning/ Practice Pattern:
Teaching : 40%
Learning : 40%
Practice : 20%

Examination Pattern:
1. Theoretical Examination: Open book / Regular Examination and on line.

Reading List:
A. Books:

Teaching Methodology

<table>
<thead>
<tr>
<th>M-Tech 2\textsuperscript{nd} Semester</th>
<th>J.C. Bose Model</th>
<th>S.N. Bose Model</th>
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<tr>
<td>Subject Code</td>
<td>Name of The Subject</td>
<td>Subject Code</td>
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<tr>
<td>ECE 907</td>
<td>DSP based System Architecture</td>
<td>ECE 905</td>
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<tr>
<td>ECE 908</td>
<td>Advanced Embedded Systems</td>
<td>ECE 906</td>
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<td>ECE 910</td>
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NAME OF THE MODULE: Micro and Nano-Fabrication Technology
Module Code: ECE 905
SEMESTER: 2\textsuperscript{nd}
Credit Value: 3 [P=0, T=0, L=3]
Module Leader: Dr. T. D. Das
No. of Lectures: 40 Hours

Objectives:
The course is designed to meet the objectives of:
1. This course introduces the theory and technology of micro/nano fabrication. Because of the interdisciplinary nature of the subject, its content includes concepts from many disciplines in engineering (electrical, materials, mechanical, chemical) and science. In lecture, we will discuss the theory of basic processing techniques, such as diffusion, oxidation, photolithography, chemical vapor deposition, physical vapor deposition, etching, and metallization.

2. In the labs section of this course, we will be fabricating three different devices; an MOS capacitor, a microcantilever, and a microfluidic device. You will test each device in the lab and prepare a laboratory report for each device.

3. At the end of this course, one should have a good understanding of the various processing techniques used to micro/nano fabricate. One should understand the theory of the individual processes, how they are characterized, and the interrelationship of these processes when combined to fabricate devices.

Learning outcomes:
At the end of this module, students are expected to be able to:
1. To develop knowledge and an understanding of micro and nano fabrication technologies, processes and their applications
2. appreciate the difference between micro- and nano-fabrication in the context of CMOS scaling
3. describe a range of nanoscale fabrication and characterisation technologies
4. demonstrate understanding of specific nanofabrication approaches
5. explain image formation in a number of high-resolution microscopies
6. identify some major issues and developments at the frontiers of nano-engineering

Subject Matter:

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<th>UNIT</th>
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<tr>
<td>UNIT I</td>
<td><strong>Introduction</strong>: Overview and comparison of micro fabrication and nano-structuring processes and applications for micro/nano technology. <strong>Equipment subsystems</strong>: Oxidation furnace , Chemical vapor deposition , Plasma etching , Ion implantation</td>
<td>8</td>
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<tr>
<td>UNIT II</td>
<td><strong>Basic Nanofabrication Processes</strong>: p-n junction diode process flow , n-p-n bipolar transistor process flow , CMOS transistor process flow , Power device process flow , MEM process flow , Biomedical device fabrication</td>
<td>8</td>
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<tr>
<td>UNIT III</td>
<td><strong>Deposition Process</strong>: Thin film deposition processes- Chemical vapor deposition (CVD) processes: Nitride deposition , Oxide deposition , Polysilicon deposition , Plasma enhanced CVD , Physical vapor deposition-sputtering , Physical vapor deposition-thermal and e-gun evaporation Etching Processes: Wet chemical etching , Plasma etching , Reactive ion etching (RIE) , High ion density reactors , Dielectrics , Polymers , MEMS deep silicon</td>
<td>12</td>
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<tr>
<td>UNIT IV</td>
<td><strong>Characterization, Packaging, and Testing of Nanofabrication Structures</strong>: Process monitoring techniques- Residual gas analysis (RGA) , Optical emission spectroscopy (OES) , Laser interferometry Surface analysis techniques- Ellipsometry , Profilometry Oxide electrical characterization; Transistor characterization ; Yield analysis techniques ; Electron Microscopy ; MEM and biomedical devices characterization and testing ; Interconnect metalization ; Planarization ; Packaging ; Reliability issues</td>
<td>12</td>
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</table>
Teaching/Learning/Practice Practice Pattern:
Teaching : 40%
Learning : 10%
Practice : 50%

Examination Pattern:
1. Theoretical Examination: Regular examination and on line test.
2. Practical Examination: Conducting Experiment and Viva-Voice.

Reading List:
A. BOOKS:

B. MAGAZINES:
1. IEEE Magazine for Consumer Electronics
2. I-Micronews
3. Magazine on Solid state Technology
5. CMM internationals

C. JOURNALS:
2. Journal of Micro / Nanolithography, MEMS and MOEMS
3. Journal of Microlithography, Microfabrication, and Microsystems
4. Microsystems Technology

NAME OF THE MODULE: MEMS and RF based IC Design
Module Code: ECE 906
SEMESTER: 2nd
Credit Value: 3 [P=2, T=0, L=3]
Module Leader: Santanu Maity
No. of Lectures: 48 Hours

Objectives:
The course is designed to meet the objectives of:
1. To gather knowledge on MEMS and its fabrication
2. To work on MEMS Simulators
3. To provide a clear foundation of Sensor design

Learning outcomes:
At the end of this module, students are expected to be able to
3. Design RF MEMS Switch for its application in different microwave frequencies.
4. Design and develop consumer products such as accelerometers used in cars to activate the airbags and in smart phones to flip images and play video games.

Subject Matter:

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<th>UNIT I</th>
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<tr>
<td><strong>Introduction:</strong> Micro sensors and MEMS, Evolution of Micro sensors &amp; MEMS, Micro sensors &amp; MEMS applications, Bulk Micromachining: wet etch-based, dissolved wafer process, SOI MEMS, Scream, Hexsil MEMS, sealed cavity deep RIE, Process Integration: interleaved, MEMS-first, MEMS-last, bonded integration, wafer-to-wafer transfer, fluidic assembly.</td>
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| UNIT II | Mechanics of Materials for MEMS: stress, strain, material properties, measurement & characterization of mechanical parameter. Microstructural Elements: bending moment and strain, flexural rigidity, residual stress, boundary conditions, spring combinations. | 10 |

| UNIT III | Energy Methods I: application to clamped-clamped beam under axial load. Energy Methods II: resonance frequency determination, free-free beam, disk, ring, lumped-element mechanical equivalent circuits | 8 |

| UNIT IV | Phase-locked loops, low voltage frequency synthesizers, printed circuit board design for RF applications. Antennas and signal propagation, design of an on-chip antenna. RF filters, oversampling (Sigma Delta) A/D converters, impact of substrate noise and other mixed-signal IC issues. RF/Analog integrated circuit design based on high frequency BiCMOS technology. | 12 |

Teaching/Learning/Practice Practice Pattern:
Teaching : 40%
Learning : 10%
Practice : 50%

Examination Pattern:
3. Theoretical Examination: Regular examination and on line test.
4. Practical Examination: Conducting Experiment and Viva-Voice.

Reading List:
A. BOOKS:
SYLLABUS FOR M-TECH. (ELECTRONICS DESIGN & MANUFACTURING)


B. MAGAZINES:
1. IEEE Magazine for Consumer Electronics
2. I-Micronews
3. Magazine on Solid State Technology
4. MEMS’ Trends: Magazine on MEMS technology and Markets
5. CMM internationals

C. JOURNALS:
2. Journal of Micro / Nanolithography, MEMS and MOEMS
3. Journal of Microlithography, Microfabrication, and Microsystems
4. Microsystems Technology
5. Microfluidics and Nanofluidics, Springer

Name of the Module: DSP Based System Architecture
Module Code: ECE 907
SEMESTER: 2nd
Credit Value: 4 [P=2, T=0, L=3]
Module Leader: Yang Saring
No. of Lectures: 42 Hours

Objectives:
1. To make the students to understand different types of digital signal processing techniques and tools
2. To make students familiarization about advanced transform, namely discrete Z transform, Fast Fourier transform and Filters using MATLAB
3. To make students to apply transform and DSP techniques to design systems of coding & decoding

Learning outcomes:
At the end of this module, students are able to
1. Utilize the DSP tools and Techniques, Discrete Z transform, Fast Fourier Transform to design system & analysis
2. To design important filters FIR, IIR for systems and analysis.

Subject Matter:

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23
| UNIT I | Introduction: Overview of digital signal processing, Multichannel and multidimensional signals, Sequences: classification based on length, symmetry, periodicity, energy, power, Discrete signal, Time linear system, Sequences, arbitrary sequences, linear time invariant system, causality, stability, Difference equation, relation between continuous and discrete system, Classifications of sequence, recursive and non-recursive system.  
Z-transform: Definition, relation between Z transform and Fourier transform of a sequence, properties of Z transform, mapping between S-plane and Z-plane, UNIT circle, convergence and ROC, Inverse z-transform, solution of difference equation using the one sided Z-transform with MATLAB examples. |
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<td>Lectures</td>
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List of Practical:

1. Generate discrete sinusoidal signal, exponential, unit step sequence, ramp sequence, impulse sequence.
2. Carry out multiple operations such as addition, Multiplication, Shifting and Folding on the above generated signal.
3. Developed a methodology to correlate signals for Aircraft.
5. Find the DFT of the above correlated signal and study the spectrum of the signal.
6. Design and implement a FIR filter, and test the filter as LPF.
7. Design and implement an IIR filter, and test the filter as LPF and compare with FIR filter.
8. Generate signals using DSP processor TMS320C64xx kit.
9. Perform sampling, quantization on DSP processor kit by integrating DSP codec & MATLAB code to study the effects of aliasing on sound signals.
10. Perform Convolution and Correlation of given signals on DSP processor kit.
Teaching/Learning/Practice Pattern
Teaching: 40%
Learning: 10%
Practice: 50%

Examination Pattern
1. Theoretical Examination: Written
2. Practical Examination: Conducting experiments and viva-voce.

Reading list:
A. BOOKS
3. Chen, “Digital Processing”, Oxford University Press,
4. Meyar-Basse U, “Digital Signal Processing with FPGA”, Springer India,

B. MAGAZINES:
2. Electronics Business Magazine.
3. IEE ASSP Magazine

C. JOURNALS:
1. IEEE journal on selected Areas in communication.
2. Springer
3. IEEE Spectrum
5. AT&T Bell Laboratory Technical Journal
6. Electronics Letter

Name of the Module: Advanced Embedded System
Module Code: ECE 908
SEMESTER: 2nd
Credit Value: 4 [P=2, T=0, L=3]
No. of Lectures: 40 Hours

Objectives:
The course is design to meet the objectives of:
1. Define the class and its goals
2. Provide a general overview of Embedded Systems and RTOS
3. Learn to design and development of an embedded system, including hardware and embedded software development.
4. Give examples of Embedded Systems
5. Show current statistics of Embedded Systems

Learning outcomes:
Upon completion of the subjects:
1. Know about Embedded systems and the interface issues related to it.
Syllabus for M-Tech. (Electronics Design & Manufacturing)

2. Know about different techniques on embedded systems
3. Know about the real time models, languages and operating systems
4. To analyze real time examples, obstacles and solutions.

Subject Matter:

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<tr>
<td>II</td>
<td>Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modeling, External peripherals – Type of memory – Memory testing , memory management. Case study.</td>
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<tr>
<td>III</td>
<td>Introduction to RTOS: OS in embedded systems, multi tasking using priority based preemptive schedulers are covered. RTOS- Inter Process communication, Interrupt driven Input and Output - Nonmaskable interrupt, Software interrupt; Thread – Single, Multithread concept; Multitasking sequential circuit Handling of interrupts in RTOS and timing analysis. Case study.</td>
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<tr>
<td>IV</td>
<td>Embedded system design, Embedded C, Role of Infinite loop instruction sequencing, Compiling, State Machine, Pattern Sequence Detector, different type of embedded multitasking sequential switching circuit design and optimization. Case study.</td>
<td>14</td>
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</table>

List of Practical:
1. Design an embedded controller for automatic room temperature control.
2. Design an embedded system for automatic washing machine.
3. Design an embedded system for auto-pilot mechanism.
4. Design an embedded system for industrial automation.
5. Design an embedded system for AUV.
6. Design an embedded system for Robot gripper.
7. Design an embedded system for wheel mechanism of mobile robot.
8. Design an embedded system for obstacle avoidance by an assembly line robot.
9. Any innovative embedded system design as mini project.

Teaching/ Learning/ Practice Pattern:

Teaching: 70%
Learning: 30%
Practice: 0%

Examination Pattern:
1. Theoretical Examination: Regular Examination

Reading List:

A. TEXT BOOK
1. GNU/Linux application programming, Jones, M Tim, Dreamtech press, New Delhi
SYLLABUS FOR M-TECH. (ELECTRONICS DESIGN & MANUFACTURING)

5. Data structures Through ‘C’ Language, Samiran Chattopadhyay, Debarata Ghosh Dastidar, Matangini Chattopadhyay, DOEACC Society
7. C and the 8051 Programming Volume II, Building efficient applications, Thomas W Schultz, Prentice hal

B. REFERENCE BOOKS:
1. UNIX NETWORK PROGRAMMING, STEVENS, W RICHARD, PH, New Jersey
2. Linux Device Drivers, 2nd Edition, By Alessandro Rubini & Jonathan Corbet, O'Reilly
3. Data Structures Using C- ISRD group, TMH
4. Data structures –Seymour Lipschutz, Schaums Outlines
5. Let us C, Yashwant Kanetkar
6. C Programming for Embedded systems, Zurell, Kirk
7. C and the 8051 Programming for Multitasking – Schultz, Thomas W
8. C with assembly language, Steven Holzner, BPB publication
9. C and the 8051: Hardware, Modular Programming and Multitasking Vol I – Schultz, Thomas W
10. Embedded C, Pont, Michael J
11. Art of C Programming, JONES, ROBIN, STEWART, IAN
13. Advanced Linux Programming Mark Mitchell, Jeffrey Oldham, and Alex Samuel,
15. P H Winston - Artificial Intelligence - Pearson Education
17. Computational Intelligence: A logical Approach, by Davin Poole, Alan Mackworth, and Randy Goebel, Oxford University Press.

C. Magazines:
1. Embedded Systems Design magazine archive, South Tower San Francisco, CA 94107
2. Embedded Innovator Newsletter and magazines, Intel, Santa Clara, CA.
3. Embedded Computing Design, Saint Clair Shores, MI 48082
4. AI Magazine - Association for the Advancement of Artificial Intelligence, AAAI Press, USA
5. IEEE Intelligent Systems Magazine, Computer Society, United State

D. Journals:
2. International Journal of Reconfigurable and Embedded Systems (IJRES), ISSN: 2089-4864, IAES

B. Journals:
1. Group and Organization Management.
3. Journal of Management
Syllabus for M.Tech. (Electronics Design & Manufacturing)

Name of the Module: Dissertation (Advanced Manufacturing & Systems Management)
Module Code: ECE 910
SEMESTER:
Credit: 5 [P=30, T=0, L=0]
Module Leader:
No. of Lectures:

Overview:
Students carry out an individual project of about three month’s duration in an area related to the preceding taught programme Units. Depending on the subject chosen, this work can be experimental in nature or can involve modelling and simulation, or can be a combination of both. The work is then written up in the form of a Dissertation

Aims:
The aim of this module is to carry out a substantial piece of research work in a specific technological area and report on this work in the form of a Dissertation.

ELECTIVE PAPER – I
(For M-Tech 2\textsuperscript{nd} Semester)

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
<th>P</th>
<th>T</th>
<th>L</th>
<th>Credit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECE 915</td>
<td>System on Chip</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>ECE 916</td>
<td>Design of Semiconductor Memories</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>ECE 917</td>
<td>Computer Architecture &amp; Parallel Processing</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>ECE 918</td>
<td>VLSI Design – II</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>ECE 919</td>
<td>Electronic Instrumentation Design</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

Name of the Module: System on Chip
Module Code: ECE 915
SEMESTER: 1st
Credit Value: 3 [P=0, T=0, L=3]
Module Leader: Abir Jyoti Mondal / Alak Majumder
No. of Lectures: 36 Hours

Objectives:
The course is designed to meet with the objectives of
1. Provide students with specialised knowledge that covers all levels of abstraction from electronic systems to the actual construction of a circuit.
2. The programme is characterised by a holistic view of circuit design which gives a qualification which is directly applicable in industry.

Learning Outcomes:
Upon Completion of the topics:
1. To gain knowledge of the data structures and algorithms used in modern logic synthesis tools
2. To learn advanced techniques for logic circuit optimization
3. To develop skills in evaluating different data structures for target applications
4. To understand merits and limitations of logic synthesis.
### Subject Matter:

<table>
<thead>
<tr>
<th>UNIT</th>
<th>COURSE CONTENT</th>
<th>Number of Lectures</th>
</tr>
</thead>
</table>
| **UNIT I** | **Introduction to Interconnection Networks:** Questions about Interconnection Networks, Uses of Interconnection Networks, Network Basic.  
**A Simple Interconnection Network:** Network Specifications and Constraints, Topology, Routing, Flow Control, Router Design, Case Study.  
Topology Basics: Nomenclature, Traffic Patterns, Performance, Case Study. | 8                  |
| **UNIT II** | **Butterfly Networks:** The Structure of Butterfly Networks, Isomorphic Butterflies, Performance, Case Study.  
**Torus Networks:** The Structure of Torus Networks, Performance, Building Mesh and Torus Networks, Case Study.  
**Non Blocking Networks:** Non Blocking vs. Non Interfering Networks, Crossbar Networks, Clos Networks. | 10                 |
**Flow Control Basics:** Resources and Allocation Units, Bufferless Flow Control, Circuit Switching, Buffered Flow Control.  
**Deadlock and Livelock:** Deadlock, Deadlock Avoidance, Adaptive Routing, Deadlock Recovery, Livelock. | 10                 |
| **UNIT IV** | **Router Architecture:** Basic Router Architecture, Router Datapath Components, Arbitration, Allocation.  
**Network Interfaces:** Process Network Interface, Shared Memory Interface.  
Buses: Bus Basics, Bus Arbitration, Bus to Network. | 8                  |

#### Teaching/Learning/Practice Practice Pattern:

- Teaching: 40%
- Learning: 10%
- Practice: 50%

#### Examination Pattern:

1. Theoretical Examination: Open book/ Regular examination and on line test.

#### READING LIST:

**A. Books:**

3. Interconnection Networks by Jose Duato, Sudhakar Yalamanchili and Lionel Ni, Morgan Kaufmann Publishers.

**B. Magazines:**

1. ACM/IEEE international symposium on networks-on-chip.
2. International Conference on VLSI and System on Chip.
3. IEEE Conferences on Very Large Scale Integration.
Syllabus for M-Tech. (Electronics Design & Manufacturing)


C. Journals:
2. IET Computer and Digital Techniques.

Name of the Module: Design of Semiconductor Memories
Module Code: ECE 916
SEMESTER: 1st
Credit Value: 3 [P=0, T=0, L=3]
Module Leader: Dr. Pinaki Chakraborty
No. of Lectures: 40 Hours

Objectives:
1. To understand how a semiconductor memory works
2. Application of SRAM, DRAM & RRAM in industry
3. To study testing and fault modeling of different types of memory

Learning Outcomes:
After finishing of this course the students will be able to -
1. Solve problems occurs in different industry graded memories.
2. Solve application specific memory testing
3. Discuss the high density memory packaging.
4. Students will be substantially prepared to take up prospective research assignments.

Subject Matter:

<table>
<thead>
<tr>
<th>Unit</th>
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<th>Number of Lectures</th>
</tr>
</thead>
</table>
| UNIT I | **SRAM:** SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies- SOI Technology-Advanced SRAM Architectures & Technologies- Application Specific SRAMs.  
**DRAM:** DRAM Technology Development-CMOS DRAMs - DRAMs Cell Theory and Advanced Cell Structures -BiCMOS, DRAMs - Soft Error Failures in DRAMs - Advanced DRAM Designs and Architecture-Application Specific DRAMs. | 10 |
| UNIT II | **ROM:** Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) -Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs) -EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture. | 10 |
### Syllabus for M-Tech. (Electronics Design & Manufacturing)

|---------|---------------------------------------------------------------------------------------------------------------|

**Teaching/Learning/Practice Practice Pattern:**
- Teaching: 40%
- Learning: 10%
- Practice: 50%

**Examination Pattern:**
1. Theoretical Examination: Open book/ Regular examination and on line test.

**Reading List:**

**A. Text Books:**

**B. Reference Books:**
1. Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.

**C. Magazines:**
2. Electron Devices magazines.

**D. Journals:**
1. IBM Journal of Research and Development.

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Name of the Module: Computer Architecture & Parallel Processing  
Module Code: ECE 917  
SEMESTER: 1st  
Credit Value: 3 [P=0, T=0, L=3]  
Module Leader:
No. of Lectures: 38 Hours

Objectives:
The course is designed to meet with the objectives of
1. The course will focus primarily on fundamental parallel computer architectures; their evaluation and the tradeoffs made in their design, but will also touch on how the machines are used.

Learning Outcomes:
Upon Completion of the topics:
1. Develop a new architectural idea and evaluate its effectiveness by implementing a simulator.
2. Write a parallel application. Study the application’s synchronization or communication behaviour.

Subject Matter:

<table>
<thead>
<tr>
<th>Unit</th>
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<th>Number of Lectures</th>
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</thead>
<tbody>
<tr>
<td>UNIT I</td>
<td><strong>Parallel Computer Models</strong>: Multiprocessors and Multi-computers – Multi-vector and SIMD Computers- PRAM and VLSI Models- Conditions of Parallelism- Program Partitioning and scheduling-program flow mechanisms- parallel processing applications- speed up performance law.</td>
<td>8</td>
</tr>
<tr>
<td>UNIT II</td>
<td><strong>Hardware Technologies</strong>: Advanced processor technology – Superscalar and vector processors- Memory hierarchy technology-Virtual memory technology- Cache memory organization- Shared memory organization. <strong>Pipelining and Superscalar Techniques</strong>: Linear pipeline processors- Non linear pipeline processors- Instruction pipeline design- Arithmetic design-Superscalar and super pipeline design- Multiprocessor system interconnects- Message passing mechanisms.</td>
<td>10</td>
</tr>
<tr>
<td>UNIT III</td>
<td><strong>Multivector and SIMD Computers</strong>: Vector Processing principle- Multivector Multiprocessors- Compound Vector processing- Principles of multithreading-fine grain multicomputer-scalable and multithread architectures – Dataflow and hybrid architectures.</td>
<td>10</td>
</tr>
<tr>
<td>UNIT IV</td>
<td><strong>Parallel Programming</strong>: Parallel programming models- parallel languages and compilers- parallel programming environments synchronization and multiprocessing modes- message passing program development- mapping programs onto multicomputer- multiprocessor UNIX design goals- MACH/OS kernel architecture-OSF/1architecture and applications.</td>
<td>10</td>
</tr>
</tbody>
</table>

Teaching/Learning/Practice Practice Pattern:
Teaching: 40%
Learning: 10%
Practice: 50%

Examination Pattern:
2. Theoretical Examination: Open book/ Regular examination and on line test.

READING LIST:

A. Text Books:
### Name of the Module: VLSI Design - II  
### Module Code: ECE 918  
### SEMESTER: 2nd  
### Credit Value: 4 [P=2, T=0, L=3]  
### Module Leader: Abir Jyoti Mondal  
### No. of Lectures: 40 Hours  

**Objectives:**

The course is designed to meet with the objectives of:

1. To understand the basics of MOS in different regions of operation and to understand how to apply proper bias voltages so as to operate as a switch or amplifier.
2. To understand the operations of CAD tools in the design and analysis of MOS circuits.

**Learning Outcomes:**

Upon completion of the topics:

1. Students will be able to bias MOS transistors depending on requirements.
2. Knowledge about operations of MOS circuits.

**Subject Matter:**

<table>
<thead>
<tr>
<th>UNIT</th>
<th>COURSE CONTENT</th>
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</tr>
</thead>
</table>
**Semiconductor Memories:** Introduction, Dynamic Random Access Memory, Static Random Access Memory, Non-volatile Memory, Flash Memory, Ferroelectric Random Access Memory. | 10 |
### UNIT II

**CMOS Operational Amplifiers:** One Stage Op amps, Two Stage Op amps, Gain Boosting, Common Mode Feedback, Stability and Frequency compensation.  
**Phase Locked Loops:** Simple PLL, Charge Pump PLLs, Non ideal Effects in PLLs, Delay Locked Loops.  

10

### UNIT III

**Switch Capacitor Circuits:** Introduction, Switched Capacitor Amplifiers, Switched Capacitor Integrators.  

10

### UNIT IV

**Noise:** Types of Noise, Representation of Noise in circuits, Noise in Single Stage Amplifiers, Noise in Differential Pairs.  
**Feedback:** General Considerations, Feedback Topologies, Effect of Loading, Effect of Feedback on Noise, Band gap Reference Nonlinearity and Mismatch: Nonlinearity, Mismatch.  

10

### List of Practical’s:

1. Study of Tanner EDA tool and to explore the operations of T Editor and S Editor.  
2. N-MOS and P-MOS transistors are taken from library and appropriate voltages is applied at gate and drain terminals to obtain the desired current versus voltage waveforms.  
3. A CMOS inverter is designed using n-MOS and p-MOS transistors and an appropriate voltage is applied at the input to verify the inverter operation.  
4. NAND and AND gates are designed using MOS transistors and an appropriate input is applied to verify the corresponding logic.  
5. NOR and OR gates are designed using MOS transistors and an appropriate input is applied to verify the corresponding logic.  
6. XOR and XNOR gates are designed using MOS transistors and an appropriate input is applied to verify the corresponding logic.  
7. Half adder and Full adder are designed using MOS transistors and an appropriate input is applied to verify the output expression.  
8. Half subtractor and Full subtractor are designed using MOS transistors and an appropriate input is applied to verify the output expression.  
9. Common Source, Common Drain and Common Gate amplifiers are designed using MOS and an appropriate voltage is applied at the input to verify their output waveforms.  
10. A basic Current Mirror is designed using MOS and its output waveform is obtained to verify the relation \( I_{out} = I_{ref} \).  
11. A Cascoded Current Mirror is designed using MOS and its output waveform is obtained to verify the minimum overdrive voltage.

### Teaching/Learning/Practice Practice Pattern:

- Teaching: 40%  
- Learning: 10%  
- Practice: 50%
Syllabus for M-Tech. (Electronics Design & Manufacturing)

Examination Pattern:
3. Theoretical Examination: Open book/ Regular examination and on line test.

READING LIST:

A. Books:
4. Design of Analog CMOS Integrated Circuits by Behzad Razavi, TMH.

B. Reference Books:

C. Magazines:
2. IEEE magazines on Semiconductor manufacturing.
4. IEEE magazines on Consumer electronics.

Journals:
5. IEEE journal of selected topics in Quantum Computing.
7. IEEE transactions on VLSI systems.
8. IEEE proceeding of Computer and Digital techniques.

Name of the Module: Electronic Instrumentation Design
Module Code: ECE 919
SEMESTER: 2nd
Credit Value: 3 [P=0, T=0, L=3]
Module Leader:
No. of Lectures: 40 Hours

Objectives:
The course is design to meet with the objectives of:

1. Imparting theoretical knowledge to the students about errors in active & passive transducers.
2. Making student competent enough to construct transducer based application specific device.
3. Giving students theoretical knowledge of inter sample error and interpolation.

Learning Outcomes:
Upon completion of the subject:
1. Students will have strong visualising capability in their mind about transducer based temperature or weather sensor.
2. Students will be able to design smart sensor busses and interface circuits.

Subject Matter:
UNIT FOR M-TECH. (ELECTRONICS DESIGN & MANUFACTURING)

<table>
<thead>
<tr>
<th>UNIT</th>
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</tr>
</thead>
<tbody>
<tr>
<td>UNIT I</td>
<td><strong>Architecture of Instrumentation scheme:</strong> Static and dynamic characteristics, errors, standards and calibration. Principle and design of various active and passive transducers. Introduction to semiconductor sensors and its applications. <strong>Electrical I/O characteristics</strong> of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion. Specifications and selection of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion. Introduction to smart sensors.</td>
<td>10</td>
</tr>
<tr>
<td>UNIT II</td>
<td>Amplification, attenuation, isolation, multiplexing, filtering, linearization, compensation, simultaneous sampling &amp; transducer excitation. Operational and Instrumentation Amplifiers. Instrumentation amplifiers and Error Budgets, Noise in low level Amplification.</td>
<td>10</td>
</tr>
<tr>
<td>UNIT IV</td>
<td>Introduction to manufacturing Processes, National and International Standards (BIS, DIN, ISO etc), Product Design Fundamentals- boards/modules, sub-systems, cabinet, user interface, Design for manufacturability, Design for testability, Creating user’s manual and maintenance manual.</td>
<td>8</td>
</tr>
</tbody>
</table>

**Teaching/ Learning/ Practice Pattern:**

Teaching: 70%
Learning: 30%
Practice: 0%

**Examination Pattern:**


**Reading List:**

**A. Text Books**

**B. Reference Books**
4. Advances in Distributed Sensor Technology; by: S.S.Iyengar, L.Prasad, Hla Min; Prentice Hall PTR.

C. MAGAZINES:
2. Magazine on sensors and measurements

C. JOURNALS:
1. International Journal of Instrumentation Science
2. Journal of Instrumentation
5. International Journal of Instrumentation, Control and Automations.