Course Curriculum for M. Tech.

In

Microelectronics & Intelligent System

Electronics & Communication Engineering

(For students admitted in 2025-26 onwards)

National Institute of Technology
Arunachal Pradesh

P.O.: Jote, Dist.: Papumpare, Arunachal Pradesh, Pin–791113
www.nitap.ac.in

1.0 Semester wise Credit point distribution

Sl. No.	Year	Credit Point
1	First	21
2	Second	19
3	Third	10
4	Fourth	15
Total Credit Point		**65**

2.0 Subject Category wise Credit point Distribution

Course Category	Sem-I	Sem-II	Sem-III	Sem-IV	Total Credit Point
Core	15	3	-	-	**18**
Elective	-	12	-	-	**12**
Lab	6	4	-	-	**10**
Academic Project	-	-	10	15	**25**
Total Credit Point	**21**	**19**	**10**	**15**	**65**

3.0 Course Structure

Ist Semester						
Sl No	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	EC-5101	Physics of Semiconductor Devices	3	0	0	3
2	EC-5102	Digital CMOS VLSI	3	0	0	3
3	EC-5103	Analog CMOS IC	3	0	0	3
4	EC-5104	Embedded System & IoT	3	0	0	3
5	EC-5105	Machine Learning	3	0	0	3
6	EC-5106	VLSI Laboratory 1	0	0	6	3
7	EC-5107	Embedded System & IoT Laboratory I	0	0	4	2
8	EC-5108	Machine Learning Laboratory	0	0	2	1
Contact Hours			15	0	12	
Total Credits						21
IInd Semester						
Sl No	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	EC-5201	Mixed Signal IC Design	3	0	0	3
2	EC-5201X	Elective 1	3	0	0	3

3	EC-5202X	Elective 2	3	0	0	3
4	EC-5203X	Elective 3	3	0	0	3
5	EC-5204X	Elective 4	3	0	0	3
6	EC-5202	VLSI Laboratory II	0	0	4	2
7	EC-5203	Embedded System & IoT Laboratory II	0	0	4	2
Contact Hours			15	0	8	
Total Credits						19
IIIrd Semester						
Sl No	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	EC-5301	Dissertation I	0	0	20	10
Contact Hours			0	0	20	
Total Credits						10
IVth Semester						
Sl No	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	EC-5401	Dissertation II	0	0	30	15
Contact Hours			0	0	30	
Total Credits						15

4.0 Elective

- Students are free to choose any subjects of their interest offered as by the department of the Institute.
- The total course has to be of 12 credits.

Sl. No	Code	Subject	L	T	P	C
1	EC-5201A	VLSI System Design	3	0	0	3
	EC-5201B	Neuromorphic Computing	3	0	0	3
	EC-5201C	Network-on-Chip	3	0	0	3
2	EC-5202A	Photonic Devices & Circuits	3	0	0	3
	EC-5202B	VLSI Signal Processing	3	0	0	3
	EC-5202C	MEMS Design	3	0	0	3
3	EC-5203A	Testing & Verification of VLSI System	3	0	0	3
	EC-5203B	Design and Layout of Plant	3	0	0	3
	EC-5203C	VLSI Technology & Fabrication	3	0	0	3
4	EC-5204A	CAD for VLSI	3	0	0	3
	EC-5204B	Memory Subsystem	3	0	0	3
	EC-5204C					

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INSTITUTE VISION

"Our vision is to impart quality technical education with strong underpinning of sound knowledge in the domain. Our approach is interactive, innovative and quintessentially holistic. Our goal is to produce imaginative entrepreneurs, technology leaders of the new millennium and researchers with a profound sense of humanistic and ethical values."

INSTITUTE MISSION

"Our mission is that of producing such Technical Engineers who will not run after jobs, but for whom jobs will run after them, and such that they will create employment and develop new technologies for a faster, sustainable and inclusive growth."

DEPARTMENT VISION

“To pursue excellence in education and research in Electronics and Communication Engineering”

DEPARTMENT MISSION

The mission of the Department of Electronics and Communication Engineering are:

- To impart strong theoretical and experimental foundation in Electronics and Communication Engineering
- To educate students with state of art technologies to meet the growing challenges of industry as well as society
- To produce and disseminate theory, principles, practice and know – how of various fields of Electronics such as Communication, signal processing, VLSI, Nanotechnology and many more in tune with the needs and demands of changing times.

Programme Outcomes (POs)

The students who have undergone the M.Tech. programme in Electronics and Communication Engineering (ECE) will be able to:

PO1	Apply basic science and mathematics to analyze complex engineering problems
PO2	Gather requirement specifications, design and test electronic systems.
PO3	Apply EDA tools to design linear and digital IC systems.
PO4	Analyze and design noise-free analog and digital VLSI systems
PO5	Evaluate strengths and weaknesses of evolving state of art VLSI systems.
PO6	Understand and practice professional ethics.
PO7	Work in a team using technical skills, common tools and environments to achieve project objective.
PO8	Communicate effectively with peers and others.

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5101	Physics of Semiconductor Devices	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**1.** To understand the physical structure and electrical properties of semiconductor materials **2.** To master the fundamental concepts and equations of semiconductor devices. **3.** To understand the terminal characteristics of junction diodes, bipolar transistors, and field-effect transistors.	**Course Outcomes**	**CO1**	To explain the principle of semiconductor physics	Knowledge
			CO2	To interpret the current voltage characteristics and mathematical model of BJT	Understand
			CO3	To apply the concept of current voltage characteristics in analyzing small signal model of transistors	Apply
			CO4	To analyze the working and characteristics of MOSFET and FET	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	3	2	0	1	0	0	0	0	0	0	1	3	2	2
2	CO2	3	3	2	0	1	0	0	0	0	0	0	1	2	2	3
3	CO3	3	3	2	0	1	0	0	0	0	0	0	1	2	2	3
4	CO4	2	2	2	0	1	0	0	0	0	0	0	1	2	2	2
(Average)		2.75	2.75	2	0	1	0	0	0	0	0	0	1	2.25	2	2.5

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Semiconductor fundamentals***: Band theory, E-k diagram, Effective mass, Density of states, Carrier density, Degeneracy, Compensation ***Transport***: Ohm's law, Mobility, Boltzmann equation, Hall mobility, Diffusion, Scattering mechanism, Hot electron ***Excess Carrier***: Recombination in direct gap, SRH theory, Traps, Continuity equation ***PN junction theory***: Band diagram of semiconductor PN junction, Depletion width, Built in potential, I-V characteristics, Varactor diode	**10**	**CO1**
II	***Bipolar junction transistor***: Minority carrier distribution and terminal currents, Generalized biasing, Switching, Secondary effects, Frequency limitation of transistor ***MOS capacitor and MOSFETs***: Band diagram under depletion, Inversion and accumulation, Threshold voltage and control, C-V curve, I-V characteristics, Gradual channel approximation, Charge sheet model, Pao Sah current formation, Subthreshold current conduction, Channel length modulation, Hot electron	**10**	**CO2, CO3**
III	***Advance MOSFET***: CMOS scaling, Short channel effects, Threshold voltage roll off, DIBL, GIDL, Gate leakage current, Hot carrier injection, Punch through, Silicon-on-insulator MOSFET, Low power high speed design issues	**10**	**CO2**
IV	***Heterostructure and quantum well devices*:** Quantization and low dimensional electron gas, Influence on MOSFET characteristics, Band alignment in Si/ SiGe heterostructures, High electron mobility transistors (HEMT), Quantum well FETs, FinFET, FDSOI, Gate all Around (GAA)	**10**	**CO3, CO4**
Total Hours			

Textbooks:

1. B. G. Streetman, S. K. Banerjee, Solid State Electronic Devices, Pearson Education, 7e, 2015.
2. D. A. Neamen, Semiconductor Physics and Devices: Basic Principles, MGH, 4e, 2012.

Reference Books:

1. S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, Wiley Eastern, 3e, 2008.
2. J. P. Colinge, C. A. Colinge, Physics of Semiconductor Devices, Kluwer Academic Publishers, 2e, 2002.
3. Kevin F. Brennan, The Physics of Semiconductors, Cambridge Univ. Press, 1999.

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Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5102	Digital CMOS VLSI	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. To understand MOS structure and working
2. To understand working of different MOS inverters and to analyze VTC
3. To understand MOS use in combinational and sequential circuits
4. To understand different interconnect, arithmetic circuits and low power techniques

Course Outcomes

CO1	To describe the MOS working and identify the difference with BJT	Knowledge
CO2	To interpret and infer MOS input output characteristics and application in circuits	Understand
CO3	To use MOS in arithmetic and logic circuit and to understand different interconnect	Apply
CO4	To analyze different low power circuit techniques	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	0	0	2	0	0	0	0	0	0	0	0	3	2	3
2	CO2	3	2	2	2	2	0	0	0	0	0	0	0	2	3	2
3	CO3	3	2	2	2	2	0	0	0	0	0	0	0	3	3	2
4	CO4	3	2	2	2	2	0	0	0	0	0	0	0	2	2	2
(Average)		3	1.5	1.5	2	1.5	0	0	0	0	0	0	0	2.5	2.5	2.25

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***MOS transistor theory***: Ideal I-V characteristics; C-V characteristics; Non ideal I-V effect; DC transfer characteristics ***Electrical wire model***: The ideal wire; the lumped model; the lumped RC model and distributed RC line ***CMOS inverter***: Static CMOS inverter; Static behaviour- Switching threshold, noise margin; Dynamic behaviour- computing capacitance, propagation delay, energy and energy delay; Dynamic, static and short circuit power; Technology scaling and its impact ***CMOS fabrication and layout***: Fabrication process; Layout design rules- stick diagram; Technology related CAD issues; Manufacturing issues; Custom to semicustom and structured array design approaches; Cell based design methodology; Array based implementation approaches	**10**	**CO1**
II	***CMOS combinational logic gates***: Static CMOS design; Ratioed logic and pass transistor logic; Dynamic CMOS design- dynamic logic, speed and power dissipation; Signal integrity issues; Logic design for reduced supply voltages ***CMOS sequential logic circuits***: Timing metrics; Static latches and registers- bistability principle; Multiplexer based latches; Master slave edge triggered register; Low voltage static latches; Dynamic latches and registers; Pipelining; Synchronous design- timing basics, sources of skew and jitter; Clock distribution approaches	**12**	**CO1, CO2**
III	***Interconnect***: Capacitive parasitics- crosstalk, capacitance; Resistive parasitics- resistance and reliability; Electromigration and RC delay; Inductive parasitics; Reduced swing circuits ***Arithmetic & logic circuits***: Adder circuits- carry look-ahead adder, carry select adder; Multipliers; Barrel shifters; General purpose functional block and ALU design	**10**	**CO3, CO4**
IV	***Low power circuits***: Leakage in nanometer technologies; Modelling for design in deep submicron technologies; Low power dynamic logic circuits; Circuit techniques for leakage reduction and clock powered circuits	**8**	**CO3, CO4**
	Total Hours	**40**	

Textbooks:

1. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits, TMH, 3e, 2012.
2. J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits, PHI, 2e, 2003.

Reference Books:

1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, Oxford University Press, 2004.
2. K. Martin, Digital Integrated Circuit Design, OUP, 1999.

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Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5103	Analog CMOS IC	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. To understand single stage and differential operation
2. To understand design and analysis of current mirror
3. To understand design and analysis of operational amplifier
4. To understand operational amplifier applications

Course Outcomes		
CO1	To identify MOS single stage and differential circuits behaviour	Knowledge
CO2	To interpret working of current mirror & operational amplifier	Understand
CO3	To relate operational amplifier working in applications	Apply
CO4	To connect and conclude operational amplifier applications	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	2	2	0	0	0	0	0	0	0	0	2	3	2
2	CO2	3	2	3	3	0	0	0	0	0	0	0	0	3	2	2
3	CO3	3	2	3	3	0	0	0	0	0	0	0	0	2	2	2
4	CO4	3	2	2	2	0	0	0	0	0	0	0	0	2	2	2
(Average)		3	2	2.5	2.5	0	0	0	0	0	0	0	0	2.25	2.25	2

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Review of MOS transistor***: MOS structure, MOS I-V characteristics, second order effects, MOS device models. ***Single stage amplifier***: Common source, Source followers, Common gate, Cascode. ***Analog CMOS sub circuits***: MOS switch, Current sink and sources, Current mirrors, Current & voltage references.	**11**	**CO1**
II	***Differential amplifier***: Single ended and differential, Basic differential pair, Common mode response, Gilbert cell ***Frequency response of amplifiers***: Miller effect, Common source stage, Source follower, Common gate, Cascode and Differential pair.	**11**	**CO1, CO2**
III	***Noise***: Characteristic, type & representation, Noise in single and differential amplifiers. ***Feedback***: Properties of feedback circuits, Types, Feedback topologies, Effect of loading. ***Oscillators***: General consideration, Ring oscillator, LC oscillator and Voltage controlled oscillator.	**10**	**CO2, CO3**
IV	***Operational amplifier***: Basic concepts, Performance parameter, One-stage opamp, Two-stage opamp, Gain boosting, Slew rate, Power supply rejection ratio, Stability and frequency compensation. ***High performance CMOS opamp***: Micro power opamp, Low noise opamp, Low voltage opamp.	**8**	**CO3, CO4**
Total Hours		**40**	

Textbooks:

1. Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 3e, Tata Mc Graw-Hill, 2007.
2. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education, 2e, 2017.

Reference Books:

1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, Oxford University Press, 7e, 2014
2. P. R. Gray, R. G. Meyer, P. J. Hurst and S. H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley International, 4e, 2005.
3. Michael Jacob, Applications and Design with Analog Integrated Circuits, Prentice Hall of India, 2e, 1996.

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Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5104	Embedded Systems and IoT	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**1.** To understand microcontrollers and the concept of embedded system **2.** To understand the operation of IoT **3.** Designing of Intelligent System	**Course Outcomes**	**CO1**	Understand microcontrollers and embedded systems — Knowledge
			CO2	Understand Real Time Operating Systems — Understand
			CO3	Interfacing and Interrupt driven input and output. — Apply
			CO4	Industrial applications — Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**MappingwithPSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	2	1	0	0	0	0	0	0	0	0	3	1	3
2	CO2	2	3	2	2	1	0	0	0	0	0	0	0	2	2	3
3	CO3	1	3	3	2	2	1	1	0	0	0	0	1	2	2	3
4	CO4	1	1	2	1	0	1	0	0	0	0	0	1	2	2	2
(Average)		1.75	2.25	2.25	1.5	0.75	0.5	0.25	0	0	0	0	0.5	2.25	1.75	2.75

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	**Review of Embedded system**: Requirements of embedded system, Hardware software co-design, architecture, challenges and design issues in embedded systems. **Review:** of 8051 design consideration and applications. **Embedded Controller Arduino Family:** Introduction and its variety, Intel Galileo, Reading data from analog and digital sensors on serial monitor/LCD monitor, Work with LED controlled by switch/potentiometer, Interfacing relays and servomotors to Arduino and Galileo.	**12**	**CO1**
II	***RTOS:*** Tasks, process and threads, Multi-processing and multi-tasking, Threads – single, multi-thread concept; multitasking multiple input multiple output and sequential operations, task synchronization techniques. Handling of interrupts in RTOS and timing analysis and applications.	**10**	**CO2 & CO3**
III	***IoT*:** Introduction to IoT Platform, Data management, cloud computing, IoT Security, IoT device energy level issues. Interfacing a sensor and Appliances control through server; Design challenges. Key challenges in IoT: security, privacy, scalability, interoperability, **Emerging trends:** AI + IoT, 5G + IoT, Digital Twins	**8**	**CO1 & CO3**
IV	Application of Embedded System in Mechatronics, Robotics and Industrial Automation	**12**	**CO1, CO2, CO3, CO4**
	Total Hours	**40**	

Textbooks:

1. James K. Peckol, Anikt A. Bhurane, Dushyant K. Sing, Lachit Dutta, Sahadev Roy, Trailokya Nath Sasamal "Embedded Systems A Contemporary Design Tool", Wiley, 378-93-5746-396-6, (2024)
2. M IA Mazidi, J G Mazidi, R D McKinlay, The 8051 Microcontroller and Embedded Systems Using Assemble and C, Pearson/Prentice Hall, 2nd Ed
3. Lyla B Das; Embedded Systems and Integrated Approach, Pearson, India, 2013, first edition,
4. Rajkamal, Microcontrollers, Archi, Progr, interfacing and Sys design, Pearson, India, 2nd ed, 2012

Reference Books:

1. Kenneth Ayala, The 8051 Microcontroller, Cengage learning, India, 2004 3rd Ed
2. K M Bhurchandi, A K Ray, Advanced microprocessors and Peripherals, McGraw Hill Education India, 2012, 3rd ed Top
3. K V Shibu, Introduction to Embedded Systems, Tata McGraw Hill Education, India, 2009

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Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5105	Machine Learning	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. To understand the fundamental principles and theory underlying machine learning.
2. learn various supervised, unsupervised, and reinforcement learning algorithms, their implementation, and comparative performance.
3. To develop the ability to formulate and model real-world problems as machine learning tasks.
4. To gain insight into advanced ML concepts including neural networks and generative models.

Course Outcomes

CO1	Identify and apply suitable ML techniques for classification, pattern recognition, and optimization problems.	Knowledge
CO2	Explain and analyze supervised learning methods including regression, SVMs, and probabilistic models.	Understand
CO3	Explain and implement unsupervised learning techniques such as clustering and dimensionality reduction.	Understand
CO4	Explain reinforcement learning concepts and generative AI applications.	Understand

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	3	2	2	2	0	0	0	0	0	0	0	3	3	2
2	CO2	3	3	3	2	2	0	0	0	0	0	0	0	3	3	2
3	CO3	3	3	3	2	2	0	0	0	0	0	0	0	3	2	2
4	CO4	3	3	3	3	2	0	0	0	0	0	0	0	3	3	2
(Average)		3	3	2.5	2.25	2	0	0	0	0	0	0	0	3	2.75	2

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Introduction***: Introduction to Machine Learning, Examples of Machine Learning applications, Types of machine learning. Generalization and regularization, Performance Measure. **Supervised Learning**: Linear Regression, Classification and Regression. **Neural Networks**: The Perceptron, Activation Functions, Training Feed Forward Network by Back Propagation, MLP. **Dimensionality Reduction**: Linear Discriminant Analysis (LDA), Principal Components Analysis (PCA)	**12**	**CO1, CO2**
II	**Probabilistic Learning**: HMM, Gaussian Mixture Models, Nearest Neighbour Methods **Support Vector Machines**: Optimal Separation, Kernels, The Support Vector Machine Algorithm	**10**	**CO2**
III	**Learning with Trees**: Entropy, Information Gain, using and constructing decision trees, CART, Applications of Trees **Reinforcement Learning**: Markov Decision Processes, Uses of Reinforcement Learning	**10**	**CO2, CO4**
IV	**Unsupervised Learning:** The *K*-Means Algorithm, Vector Quantisation, Hierarchical Clustering Methods, Density based clustering	**8**	**CO3**
V	**Generative AI, applications of AI ML**	**5**	**CO4**
	Total Hours	**45**	

Textbooks:

1. T. Mitchell, Machine Learning, McGraw Hill, 2017.
2. R. O. Duda, P. E. Hart, D. G. Stork, Pattern classification, Wiley, New York, 2/e, 2007.
3. Stephen Marsland, Machine Learning an algorithmic perspective, 2nd ed., CRC Press, Taylor & Francis Group, 2015

Reference Books:

1. Christopher M. Bishop, *Pattern Recognition and Machine Learning*, Springer, 2011 edition
2. Ian Goodfellow, Yoshua Bengio, Aaron Courville, *Deep Learning*, MIT Press, 2016

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**Attend.**	**Exam**	**Viva**	**Total**	**Bloom's taxonomy**
EC-5106	VLSI Laboratory I	**0**	**0**	**6**	**3**	**20**	**50**	**30**	**100**	

Course Objectives

1. To interpret CMOS inverter working and how to design basic gates, adders, latches.
2. To understand design and analysis of current mirror
3. To understand design and analysis of operational amplifier
4. To understand operational amplifier applications

Course Outcomes

CO1	To describe CMOS working and infer parameter dependencies	Knowledge
CO2	To interpret working of basic gates, adders, latches using CMOS logic and TG and relate	Understand
CO3	To relate working of current mirror & operational amplifier	Apply
CO4	To connect and conclude operational amplifier applications	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	2	2	0	0	0	0	0	0	0	0	2	3	2
2	CO2	3	2	3	3	0	0	0	0	0	0	0	0	3	2	2
3	CO3	3	2	3	3	0	0	0	0	0	0	0	0	2	2	2
4	CO4	3	2	2	2	0	0	0	0	0	0	0	0	2	2	2
(Average)		3	2	2.5	2.5	0	0	0	0	0	0	0	0	2.25	2.25	2

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Design and layout of static CMOS inverter, NAND and NOR. Design and layout of conventional master-slave D latch and flipflop. Design and layout of TG, TG based multiplexer and demultiplexer.	**40**	**CO1, CO2, CO3, CO4**
II	Design and layout of 1bit comparator, adder, subtractor and priority encoder		
III	Mini Project - ALU		
IV	Mini Project - FIFO		
V	Mini Project – Datapath		
Total Hours		**40**	

Textbooks:

1. Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 3e, Tata Mc Graw-Hill, 2007.
2. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education, 2e, 2017.

Reference Books:

1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, Oxford University Press, 7e, 2014
2. P. R. Gray, R. G. Meyer, P. J. Hurst and S. H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley International, 4e, 2005.
3. Michael Jacob, Applications and Design with Analog Integrated Circuits, Prentice Hall of India, 2e, 1996.

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**AcademicYearofRegulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**CourseName**	**CreditStructure**					**MarksDistribution**			
		L	**T**	**P**	**C**	**Attend.**	**Exam**	**Viva**	**Total**	**Bloom's taxonomy**
EC-5107	Embedded Systems & IoT Laboratory I	**0**	**0**	**4**	**2**	**20**	**50**	**30**	**100**	

Course Objectives

1. Implement and test numerical programs on assembly and Embedded C and IDE platform.
2. Interface simple peripherals like Keys, LED's, etc. with loading considerations.
3. Complete Embedded System product with different actuators and sensors.
4. Application of 5G/6G IoT

Course Outcomes

CO1	Able to understand the need of embedded systems and integrated product design procedure and role of embedded systems in various engineering fields.	Knowledge
CO2	Able to understand the appropriate selection of actuators and different control methodology for different types of real life applications.	Understand
CO3	Able to understand the various types of microcontrollers, sensors and transducers and acquire the knowledge on different types of instrumentation systems.	Apply
CO4	Able to design and develop innovative solution for real life applications in various engineering fields.	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**MappingwithPSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1.	CO1	1	1	1	1	1	1	1	1	2	2	1	2	2	1	1
2.	CO2	2	2	1	1	1	1	1	1	1	1	2	1	1	2	1
3.	CO3	1	1	1	1	1	2	1	2	1	1	2	1	1	1	1
4.	CO4	1	1	1	2	2	1	3	1	2	1	1	1	1	1	2
(Average)		1.25	1.25	1	1.25	1.25	1.25	1.5	1.25	1.5	1.25	1.5	1.25	1.25	1.25	1.25

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	1. Write an assembly language program to toggle the any port output using Keil software. 2. Write an assembly language program to interface LED with 8051 microcontroller using Keil software.	**6**	**CO1**
II	1. Write an assembly language program and Embedded C program to interface stepper motor 2. Write an assembly language program and Embedded C program to interface servo 3. Write an assembly language program to interface DC motor 4. Application of microcontroller as switches and timers	**6**	**CO1 & CO2**
II	5G IoT programming and applications	**6**	**CO1 & CO3**
IV	Complete case study/mini project using any advance microcontroller and 5G/6G IoT	**6**	**CO3 & CO4**
	Total Hours	**24**	

Textbooks:

1. James K. Peckol, Anikt A. Bhurane, Dushyant K. Sing, Lachit Dutta, Sahadev Roy, Trailokya Nath Sasamal "Embedded Systems A Contemporary Design Tool", Wiley , 378-93-5746-396-6, (2024)
2. M A Mazidi, J G Mazidi, R D McKinlay, The 8051 Microcontroller and Embedded Systems Using Assemble and C, Pearson/Prentice Hall, 2nd Ed
3. Lyla B Das; Embedded Systems and Integrated Approach, Pearson, India, 2013, first edition,
4. Rajkamal, Microcontrollers, Archi, Progr, interfacing and Sys design, Pearson, India, 2nd ed, 2012

Reference Books:

1. Kenneth Ayala, The 8051 Microcontroller, Cengage learning, India, 2004 3rd Ed
2. K M Bhurchandi, A K Ray, Advanced microprocessors and Peripherals, McGraw Hill Education India, 2012, 3rd ed Top
3. K V Shibu, Introduction to Embedded Systems, Tata McGraw Hill Education, India, 2009

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CURRICULUM

Programme	M. Tech Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**I**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**Attend.**	**Exam**	**Viva**	**Total**	**Bloom's taxonomy**
EC-5108	Machine Learning Laboratory	**0**	**0**	**2**	**1**	**20**	**50**	**30**	**100**	

Course Objectives	1. To become familiar with data and visualize univariate, bivariate, and multivariate data using statistical techniques and dimensionality reduction. 2. Implement the machine learning concepts and algorithms in any suitable language of choice.	**Course Outcomes**	**CO1**	Implement and demonstrate ML algorithms — Apply
			CO2	Evaluate different algorithms. — Evaluate
			CO3	
			CO4	

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	3	0	0	0	0	0	0	0	0	0	3	3	0	1
2	CO2	3	3	0	0	0	0	0	0	0	0	0	3	3	0	1
3	CO3	3	3	1	1	0	0	0	0	0	0	0	3	3	0	1
4	CO4	3	3	1	1	0	0	0	0	0	0	0	3	3	0	1
(Average)		3	3	0.5	0.5	0	0	0	0	0	0	0	3	3	0	1

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Develop a program to create histograms for all numerical features and analyze the distribution of each feature. Generate box plots for all numerical features and identify any outliers	**2**	**CO1**
II	Write a Python program to implement Simple Linear Regression and plot the graph.	**2**	**CO1**
III	Develop a program to demonstrate the working of Logistic Regression and show the confusion matric and show the results.	**2**	**CO1 CO2**
IV	Develop a program to implement k-Nearest Neighbour algorithm to classify the randomly generated datapoints or you may select appropriate data set for your experiment and draw graphs. Vary the value of K and compare the results.	**2**	**CO1 CO2**
V	Develop a program to implement LDA for reducing the dimensionality.	**2**	**CO1 CO2**
VI	Develop a program to implement Principal Component Analysis (PCA) for reducing the dimensionality of the Iris dataset.	**2**	**CO1 CO2**
VII	Implement Support Vector Machine for a dataset and compare the accuracy by applying the following kernel functions: i. Linear ii. Polynomial iii. RBF	**2**	**CO1 CO2**
VIII	Write a program to demonstrate the working of the decision tree based ID3 algorithm. Use an appropriate data set for building the decision tree and apply this knowledge to classify a new sample.	**2**	**CO1 CO2**
IX	Develop a program to implement k-means clustering using a dataset of your choice. Vary the number of k values as follows and compare the results	**2**	**CO1 CO2**
X	Develop an artificial neural network that would work as logic gates.	**2**	**CO1 CO2**
	Total Hours	**20**	

Textbooks:

1. Tom Mitchell, *Machine Learning*, McGraw Hill , 1997, ISBN 0-07-042807-7
2. Richard O. Duda, Peter E. Hart, David G. Stork, *Pattern classification*, Wiley, (2nd edition). Wiley, New York, 2001
3. Stephen Marsland, Machine Learning an algorithmic perspective, 2nd ed., CRC Press, Taylor & Francis Group, 2015

Reference Books:

1. Christopher M. Bishop, *Pattern Recognition and Machine Learning*, Springer, 2011 edition
2. Ian Goodfellow, Yoshua Bengio, Aaron Courville, *Deep Learning*, MIT Press , 2016

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5201	Mixed Signal IC Design	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**1.** To understand switched capacitor circuits design and working **2.** To understand design and analysis of analog filter **3.** To understand design and analysis of PLL **4.** To understand data converter	**Course Outcomes**	**CO1**	To identify switched capacitor circuit design — Knowledge
			CO2	To interpret working of analog filter — Understand
			CO3	To relate PLL working — Apply
			CO4	To connect and conclude data converters — Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	2	2	0	0	0	0	0	0	0	0	2	3	2
2	CO2	3	2	3	3	0	0	0	0	0	0	0	0	3	2	2
3	CO3	3	2	3	3	0	0	0	0	0	0	0	0	2	2	2
4	CO4	3	2	2	2	0	0	0	0	0	0	0	0	2	2	2
(Average)		3	2	2.5	2.5	0	0	0	0	0	0	0	0	2.25	2.25	2

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Switched capacitor circuits***: Switched capacitor amplifier, Integrator, Z domain model of two-phase switched capacitor circuits, 1st and 2nd order switched capacitor circuits, Switched capacitor filter.	**11**	**CO1**
II	***Analog filter design***: Bilinear transfer function and frequency, Cascade design with 1st order circuit, Biquad circuit, Butterworth low pass filter, bandpass filter, Chebyshev response, Frequency transformations, High pass and band elimination filter, Ladder design, Leapfrog simulation of ladders.	**11**	**CO1, CO2**
III	***Phase locked loop***: Revision of VCO, Simple PLL, Charge pump PLL, Nonideal effects in PLL, Delay locked loop.	**10**	**CO2, CO3**
IV	***Data converter***: Ideal D/D converter, Ideal A/D converter, Serial and flash D/A and A/D converters, Medium and high-speed converters, Over sampling converters, Performance limitation.	**8**	**CO3, CO4**
Total Hours		**40**	

Textbooks:

1. M. E. Van Valkenburg and Rolf Schaumann, Design of Analog Filters, OUP, 2e, 2011.
2. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education, 2e, 2017.
3. B. Razavi, Design of CMOS PLL, Cambridge University Press, 2020.

Reference Books:

1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, Oxford University Press, 7e, 2014
2. P. R. Gray, R. G. Meyer, P. J. Hurst and S. H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley International, 4e, 2005.
3. Michael Jacob, Applications and Design with Analog Integrated Circuits, Prentice Hall of India, 2e, 1996.

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Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5201A	VLSI System Design	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**1.** To understand basics of system hardware, programmable logic devices **2.** To understand design and analysis of synchronous, asynchronous circuits and memories **3.** To understand clock distribution in design and analysis FIFO and Network-on-Chip **4.** To understand datapath and control in processor design	**Course Outcomes**	**CO1**	To identify basics of system hardware design and programmable logic devices — Knowledge
			CO2	To interpret design using basic building blocks, synchronous and asynchronous circuits — Understand
			CO3	To relate clock distribution in Network-on-Chip and FIFO design — Apply
			CO4	To connect and conclude datapath & control in processor design — Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	2	2	0	0	0	0	0	0	0	0	2	3	2
2	CO2	3	2	3	3	0	0	0	0	0	0	0	0	3	2	2
3	CO3	3	2	3	3	0	0	0	0	0	0	0	0	2	2	2
4	CO4	3	2	2	2	0	0	0	0	0	0	0	0	2	2	2
(Average)		3	2	2.5	2.5	0	0	0	0	0	0	0	0	2.25	2.25	2

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Basics of system hardware design***: Hierarchical design using top down and bottom-up methodology, System partitioning techniques, Interfacing between system components. ***Programmable logic devices***: FPGA, CPLD, PLA, PAL. ***Design phases***: Design, Testing, Fabrication, packaging, Abstraction and types. ***Computer aided design***: Modeling & simulation, VLSI design flow, ASIC design flow.	**11**	**CO1**
II	***Designing basic building blocks***: Digital system design using conventional components such as gates, flipflops, PALs, FPGAs ***Synchronous and asynchronous circuits***: Concept of finite state machine, Moore and Mealy machines, Synchronous FSM design, State diagram, state assignment, Derivation of next state and output expressions, Arithmetic logic design, Designing multi data path ALU, Algorithmic state machine. ***Memories***: Introduction to different types of memories, Single and multiport memories. ***Introduction to globally asynchronous locally synchronous***	**11**	**CO1, CO2**
III	***Introduction to Network-on-Chip***. ***Introduction to FIFO and designing fast FIFOs***. ***Clocks***: Static timing analysis, Handling multiple clock domains, Global and local clock distribution.	**10**	**CO2, CO3**
IV	***Processor design***: Von Neumann architecture, Harvard architecture ***Datapath & control***: Enhancing performance with pipelining, Exploiting memory hierarchy. Concept of near memory computing and in-memory computing. ***x86 microprocessor architecture***: Hardware of 186, 286,386, 486 and Pentium processors with architectural evolutions, IO and Memory Interfacing	**8**	**CO3, CO4**
Total Hours		**40**	

Textbooks:

1. M. Morris Mano, Digital Logic & Computer Design, Pearson Education India, 1e, 2016.
2. S. Brown and Z. Vranesic, Digital Logic Design with Verilog, McGraw Hill Higher Education, 2002.
3. D. A. Patterson and J. L. Hennessy, Computer Organization and Design: The Hardware / Software Interface, Morgan Kaufmann, 2007.

Reference Books:

1. J. Rabey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits- A Design Perspective, Pearson, 2e, 2011.

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Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5201B	Neuromorphic Computing	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**1.** Understand neurobiological inspiration and computational neuron/synapse models. **2.** Study hardware technologies for neuromorphic systems (analog, digital, memristive). **3.** Learn neuromorphic architectures, sensors, and SNN algorithms. **4.** Evaluate neuromorphic systems for real-world edge and AI applications.	**Course Outcomes**	**CO1**	Describe neuron and synapse models and spiking network behaviour. — Knowledge
			CO2	Compare device and circuit technologies for neuromorphic systems. — Understand
			CO3	Design and simulate simple neuromorphic circuits/systems. — Apply
			CO4	Evaluate neuromorphic architectures and platforms for applications. — Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	0	0	0	0	0	0	0	0	0	0	3	2	0
2	CO2	3	3	2	0	0	0	0	0	0	0	0	0	3	2	0
3	CO3	2	3	3	2	0	0	0	0	0	0	0	0	3	3	0
4	CO4	2	3	3	3	2	0	0	0	0	0	0	0	3	3	2
(Average)		2.5	2.75	2	1.25	0.5	0	0	0	0	0	0	0	3	2.5	0.5

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Introduction & biological inspiration; Motivation for brain-inspired computing: efficiency, parallelism, event driven; Neuron & synapse basics, spiking verses rate models.	**10**	**CO1**
II	Device and circuit building blocks; Analog VLSI neurons (sub-threshold MOSFETs), memristor/MTJ synapses; CMOS, hybrid analog/digital neuromorphic chips. Neuromorphic algorithms & spiking networks; Leaky integrate-and-fire, Izhikevich models, STDP, reservoir computing; Conversion from ANN to SNN, hardware-aware learning.	**10**	**CO2**
III	Sensors and front-end integration; Event-based vision sensors (DVS), neuromorphic auditory sensors; Edge computing and neuromorphic interfaces. Architectures & implementation platforms; Neuromorphic platforms: Intel Loihi, IBM TrueNorth, SpiNNaker; research platforms in analog/memristor; Integration, system-level trade-offs (latency, power, scalability).	**10**	**C03**
IV	Applications & case-studies; Robotics, IoT, biomedical sensors, autonomous systems; Student project presentations: design/simulate a neuromorphic module. Future trends & open research; Emerging devices (spintronics, photonics), neuromorphic computing in brain-machine interfaces, ethics of brain-inspired AI.	**10**	**C04**
Total Hours		**40**	

Textbooks:

1. C. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley.
2. A. Indiveri & S.–C. Liu, *Memory and Computation in Neuromorphic Systems*, Kluwer Academic, 2015.
3. M. Davies (ed.), *"Loihi: A Neuromorphic Many Core Processor with On-Chip Learning"*, IEEE Micro special issue, 2018.

Reference Books:

1. Hasler, J. & Marr, B., "Finding a roadmap to achieve large neuromorphic hardware systems," *Frontiers in Neuroscience*, 2013.
2. P. Date et al., "Neuromorphic Computing is Turing-Complete," arXiv preprint, 2021.
3. Papers/handouts from research labs (e.g., NeuRonICS Lab at IISc) on neuromorphic CMOS/MoS_2 hybrid systems.

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Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5201C	Network-on-Chip	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. Introduce NoC fundamentals, topologies, and switching.
2. Study router architecture, flow control, and routing algorithms.
3. Analyze performance, QoS, and power/reliability in NoCs.
4. Design and simulate NoC configurations for SoC applications.

Course Outcomes

CO1	Explain NoC building blocks and flow control.	Knowledge
CO2	Analyze routing algorithms and tradeoffs.	Understand
CO3	Evaluate NoC performance and propose optimizations.	Apply
CO4	Design and simulate NoC-based application mappings.	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	0	0	0	0	0	0	0	0	0	0	3	2	0
2	CO2	3	3	2	0	0	0	0	0	0	0	0	0	3	3	0
3	CO3	3	3	3	2	0	0	0	0	0	0	0	0	3	3	2
4	CO4	3	3	3	3	2	0	0	0	0	0	0	0	3	3	2
(Average)		3	2.75	2	1.25	0.5	0	0	0	0	0	0	0	3	2.75	1

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Introduction to SoC communication challenges, need for NoC, basic concepts	**6**	**CO1**
II	NoC topologies (mesh, torus, tree), link design and modeling Switching and flow control mechanisms (wormhole, virtual cut-through, credit-based)	**12**	**CO1, CO2**
III	Router architecture: buffers, crossbar, arbitration, virtual channels Routing algorithms: deterministic, adaptive, deadlock avoidance, fairness	**12**	**CO2**
IV	Performance metrics and evaluation techniques (latency, throughput, power) QoS, reliability, and low-power techniques (fault-tolerant routing, DVFS)	**6**	**CO3**
V	Application mapping and design methodologies (MPSoC, DNN accelerators) Emerging trends: 3D-NoC, optical/photonic NoCs, reconfigurable networks	**6**	**CO4**
	Total Hours	**42**	

Textbooks:

1. W. J. Dally and B. Towles, Principles and Practices of Interconnection Networks, Morgan Kaufmann, 2004.
2. L. Benini and G. De Micheli, *Networks on Chips: Technology and Tools*, Morgan Kaufmann, 2007.

Reference Books:

1. J. Duato, S. Yalamanchili, and L. Ni, *Interconnection Networks: An Engineering Approach*, Morgan Kaufmann, 2003..
2. T. Bjerregaard and S. Mahadevan, "A Survey of Research and Practices of Network-on-Chip," *ACM Computing Surveys*, 2006.

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5202A	Photonic Devices & Circuits	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**1.** To understand the fundamental concepts of guided-wave photonics and photonic integrated circuits (PICs). **2.** To design and simulate passive and active photonic devices used in communication and sensing. **3.** To study material platforms, fabrication, and integration processes for photonic devices. **4.** To analyze applications of photonic integrated circuits (PICs) in communication, sensing, and emerging quantum technologies.	**Course Outcomes**	**CO1**	Explain waveguide modes, dispersion, coupling, and resonator behavior in photonic integrated circuits. — Knowledge
			CO2	Design and simulate passive photonic components and evaluate their performance. — Understand
			CO3	Model active photonic components and analyze performance characteristics — Apply
			CO4	Compare photonic material platforms and assess suitability for specific applications. — Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	2	2	0	0	0	0	0	0	0	0	2	3	2
2	CO2	3	2	3	3	0	0	0	0	0	0	0	0	3	2	2
3	CO3	3	2	3	3	0	0	0	0	0	0	0	0	2	2	2
4	CO4	3	2	2	2	0	0	0	0	0	0	0	0	2	2	2
(Average)		3	2	2.5	2.5	0	0	0	0	0	0	0	0	2.25	2.25	2

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Introduction to Integrated Photonics • Why integrated photonics? Applications in telecom, datacom, sensing, quantum tech. Integrated Optical Waveguides • Slab and channel waveguides (symmetric & asymmetric); Analytical methods (effective index, Marcatilli's method); Numerical analysis of 2D and 3D waveguides	**8**	**CO1**
II	Coupled-Mode Theory • Directional couplers, Mach-Zehnder interferometers, grating devices Supermode Analysis & Tapers • Y-junctions, mode splitters, combiners Loss Mechanisms in Waveguides • Scattering, absorption, radiation loss, measurement	**8**	**CO2, CO3**
III	Passive Devices • Wavelength-division multiplexers, arrayed waveguide gratings; Multimode interferometers, Bragg gratings; Integrated delay lines, Fabry–Perot, microring resonators Active Devices • Electro-optic modulators (RF design, high-speed performance); Acousto-optic, magneto-optic devices; Optical switches and filters Optical Coupling • Grating couplers, prism couplers, mode converters	**8**	**CO2, CO3**
IV	Materials & Processes • Glass, lithium niobate, silicon, III–V semiconductors, polymers; Fabrication: lithography, ion exchange, deposition, diffusion; Device characterization techniques	**8**	**CO2, CO3**
V	Resonators & Periodic Media • Bragg reflectors, photonic crystals, sub-wavelength structures III–V Optoelectronic Integrated Circuits • Transmitters, receivers, detectors Silicon Photonics • Passive and active silicon devices; Integration with electronics Emerging Directions • MEMS-photonics integration; Quantum photonics & cryptography; Future applications in AI, sensing, and communications	**8**	**CO4**
	Total Hours	**40**	

Textbooks:

1. K. Okamoto, *Fundamentals of Optical Waveguides*, Academic Press, 2006.
2. S. L. Chuang, *Physics of Photonic Devices*, Wiley, 2009.
3. C. R. Pollock & M. Lipson, *Integrated Photonics*, Kluwer, 2003.

Reference Books:

1. H. Nishihara, M. Haruna, T. Suhara, *Optical Integrated Circuits*, McGraw-Hill, 1988.
2. R. G. Hunsperger, *Integrated Optics: Theory and Applications*, Springer, 2002.
3. Richard Osgood Jr., Xiang Meng, *Principles of Photonic Integrated Circuits*, Springer Nature, 2021.

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			**Bloom's taxonomy**
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	
EC-5202B	VLSI Signal Processing	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. To introduce the fundamentals of digital signal processing systems and their realization in VLSI.
2. To understand design methodologies such as pipelining, parallel processing, unfolding, folding, and retiming for efficient DSP architectures.
3. To develop the ability to design and analyze systolic architectures and low-power DSP systems.
4. To understand and implement fast convolution, algorithmic strength reduction, and recursive/adaptive filter architectures.
5. To explore bit-level and redundant arithmetic architectures for VLSI-based signal processing applications.

Course Outcomes

CO1	Explain DSP system representations and VLSI constraints for signal processing algorithms.	Knowledge
CO2	Apply techniques like pipelining, parallel processing, retiming, unfolding, and folding for architectural optimization.	Understand
CO3	Design and implement systolic architectures, fast convolution structures, and parallel/adaptive filters.	Apply
CO4	Analyze and evaluate scaling, round-off noise, and bit-level arithmetic architectures in VLSI signal processing.	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	1	1	2	0	0	0	0	1	0	0	3	2	1
2	CO2	2	3	2	1	3	0	0	0	0	1	0	0	3	3	2
3	CO3	2	2	3	3	3	1	0	0	0	1	0	0	3	3	3
4	CO4	1	2	3	3	2	1	0	0	0	1	0	0	3	3	3
(Average)		2	2.25	2.25	2	2.5	0.5	0	0	0	1	0	0	3	2.75	2.75

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Introduction to digital signal processing systems*:** Typical DSP algorithms, DSP application demands and scaled CMOS technologies, Representations of DSP algorithms. ***Iteration bound*:** Data flow graph representation, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of multirate data flow graphs. ***Pipelining and parallel processing*:** Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power.	**10**	**CO1, CO2**
II	***Retiming*:** Definition and properties, Solving system of equalities, Retiming techniques. ***Unfolding*:** Algorithm for unfolding, Properties of unfolding, Critical path, Unfolding and retiming, Applications. ***Folding*:** Folding transformation, Register minimization techniques, Register minimization in folded architectures, Folding of multirate systems. ***Systolic architecture design*:** Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Systolic design for space representations containing delays.	**10**	**CO2, CO3**
III	***Fast convolution*:** Cook Toom, Winograd and Iterated algorithm, Cyclic Convolution. ***Algorithmic strength reduction in filters and transforms*:** Parallel FIR filters, DCT and inverse DCT, Parallel architectures for rank order filters. ***Pipelined and parallel recursive and adaptive filters*:** Pipeline interleaving in digital filters, Pipelining in 1st order IIR digital filters, Pipelining in high order IIR digital filters, Parallel processing for IIR filters, Low power IIR filter design using Pipelining and parallel processing, Pipelined adaptive digital filters.	**9**	**CO3**
IV	***Scaling and round off noise:*** State variable description of digital filters, Scaling and roundoff noise computation, Roundoff noise in pipelined IIR filters, Roundoff noise computation using state variable description. ***Digital Lattice Filter Structures*:** Digital basic lattice filters, Derivation of one multiplier, Normalized, Scaled normalized lattice filter, Roundoff noise calculation, Pipelining of lattice IIR digital filter. ***Bit Level Arithmetic Architectures*:** Parallel multipliers, Bit serial multipliers, Bit serial filter design, Distributed arithmetic. ***Redundant Arithmetic*:** Subexpression elimination, Multiple constant multiplication, Additive and multiplicative number splitting.	**8**	**CO4**
Total Hours		**37**	

Textbooks:

1. K. K. Parhi, "VLSI Digital Signal Processing and Systems, Design and Implementation", John Wiley, 1999.
2. U. Meyer Baese, "Digital Signal Processing with FPGA", 3/e, Springer, 2007.

Reference Books:

1. S. Ramachandran, "Digital VLSI Systems Design", Springer 2007.
2. K. Madisetti, "VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis", IEEE Press 1995.

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5202C	MEMS Design	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. To introduce the fundamental concepts and evolution of MEMS and microsystem technologies.
2. To understand the working principles of microsensors and microactuators along with their applications.
3. To familiarize with materials, fabrication, and micromachining techniques used in MEMS.
4. To develop the ability to interface MEMS devices with electronic circuits and understand signal conditioning methods.
5. To equip students with knowledge to design and analyze MEMS-based systems for smart applications.

Course Outcomes

CO1	Explain the fundamental principles, evolution, and classification of MEMS and microsystems.	Knowledge
CO2	Understand the working mechanisms of microsensors and microactuators, and identify their applications.	Understand
CO3	Apply knowledge of materials, micromachining, and fabrication techniques in MEMS design.	Apply
CO4	Analyze and design electronic interfacing and signal conditioning circuits for MEMS devices.	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	1	0	1	0	0	0	0	1	0	0	3	2	1
2	CO2	2	3	2	1	2	0	0	0	0	1	0	0	3	3	2
3	CO3	2	2	3	3	3	1	0	0	0	1	0	0	3	3	3
4	CO4	1	2	3	3	3	1	0	0	0	1	0	0	3	3	3
(Average)		2	2.25	2.25	1.75	2.25	0.5	0	0	0	1	0	0	3	2.75	2.25

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Overview of MEMS and Microsystems*:** Introduction, Evolution of MEMS, Microfabrication, Typical MEMS, Microsystems products and their applications, Introduction to smart materials and systems.	**5**	**CO1**
II	***Working principles of MEMS and Microsystems*:** Introduction to microsensors and microactuators, Electrical and mechanical concepts in MEMS, Sensing techniques for MEMS piezoresistive, Piezoelectric, Capacitive and Optical sensing methods, Piezoresistive sensor materials, piezoelectric materials, Applications for tactile, flow, inertia and pressure sensors, Microactuation techniques for MEMS: Actuation methods using thermal forces, piezoelectric crystals and electrostatic forces, Examples of MEMS based microsensors and microactuators.	**12**	**CO2**
III	***Microsystems materials*:** Substrates and wafers, active substrate materials, Gallium Arsenide, Quartz, piezoelectric crystals. ***Fabrication processes*:** Silicon wafer processing, Thin film deposition, Photolithography, Diffusion, Ion Implantation, Oxidation, Chemical Vapor Deposition, Physical vapor deposition – Sputtering, Deposition by Epitaxy, Etching Techniques, packaging materials. ***Micromachining processes*:** Bulk Micromachining and Surface Micromachining, the LIGA Process, other moulding techniques, Introduction to soft lithography and thick film processing, Overview of polymers in MEMS, MEMS for RF Applications.	**12**	**CO3**
IV	***Electronic circuits for MEMS and Microsystems Semiconductor devices*:** Interface electronics for MEMS, Overview of Diodes, BJT, MOSFET, CMOS, Electronic amplifiers, Operational amplifiers, Differential amplifiers, Wheatstone Bridge circuits for measurement of resistance and analog to digital converters for MEMS and Microsystems, Signal conditioning for Microsystems devices, Differential charge measurement, switched capacitor circuits for capacitance measurement, Control and Microsystems, Smart sensors and MEMS, MEMS Simulators.	**16**	**CO4**
Total Hours		**45**	

Textbooks:

1. T. R. Hsu, "MEMS and Microsystems Design and Manufacture", 1/e, Tata McGraw-Hill, 2017.
2. S. D. Senturia, "Microsystem Design", 1/e, Springer, 2003.
3. M. J. Madou, "Fundamentals of Microfabrication: The Science of Miniaturization", 2/e, CRC Press, 2018.

Reference Books:

1. C. Liu, "Foundations of MEMS", Pearson, 2011.
2. N. Maluf, "An Introduction to Microelectromechanical Systems Engineering", 2/e, Artech House, 2000.
3. J. W. Gardner, "Microsensors: Principles and Applications", Wiley, 1994.

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			**Bloom's taxonomy**
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	
EC-5203A	Testing & Verification of VLSI System	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. To understand the fundamentals of VLSI testing, verification, and validation methodologies.
2. To study fault modeling, simulation, and test generation techniques.
3. To explore automatic test pattern generation (ATPG) and scan design approaches.
4. To introduce formal verification techniques such as model checking for VLSI systems.

Course Outcomes

CO1	Explain VLSI testing needs, challenges, and fault models in IC design.	Knowledge
CO2	Apply logic simulation, fault simulation, and ATPG techniques to verify designs.	Understand
CO3	Analyze sequential ATPG, scan-based testing, and formal verification concepts.	Apply
CO4	Evaluate memory testing, BIST, and boundary scan strategies for real-world systems.	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	1	1	2	0	0	0	0	0	0	0	3	2	1
2	CO2	2	3	2	2	3	0	0	0	0	0	0	0	3	3	2
3	CO3	2	3	3	3	3	1	0	0	0	0	0	0	3	3	3
4	CO4	1	2	3	3	2	1	0	0	0	0	0	0	3	3	3
(Average)		2	2.5	2.25	2.25	2.5	0.5	0	0	0	0	0	0	3	2.75	2.75

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Course introduction, VLSI design flow, Need of pre-silicon verification and post-silicon validation and debug, VLSI testing needs and challenges, Test challenges, Yield, and Defects, Faults and fault models, Yield and fault equivalence.	**10**	**CO1**
II	Combinational equivalence checking, BDD operations and SAT, Logic simulation, Fault simulation, Deductive and concurrent fault simulation, Combinational equivalence checking, Automatic test pattern generation (ATPG): algebraic method.	**10**	**CO2**
III	D algorithm, PODEM, PODEM, FAN, Sequential equivalence checking, Sequential ATPG, Sequential equivalence checking, Sequential equivalence checking, Scan design, Sequential equivalence checking.	**10**	**CO3**
IV	Model checking, Issues in scan design, Random access scan, Basics of model checking, Partial scan, LTL & CTL, Bist, Boundary scan. Memory fault models, Memory Bist.	**10**	**CO4**
Total Hours		**40**	

Textbooks:

1. M. L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits", Springer, 2009.
2. H. Fujiwara, "Logic Testing and Design for Testability", MIT Press, 1985.
3. M. Abramovici, M. Breuer, and A. Friedman, "Digital System Testing and Testable Design", 1/e, Jaico Publishing House, 2001.

Reference Books:

1. M. Huth and M. Ryan, "Logic in Computer Science- Modelling and Reasoning about Systems", 2/e, Cambridge Univ. Press, 2005.
2. T. Kropf, "Introduction to Formal Hardware Verification", 1/e, Springer, 2010.
3. M. Bushnell, Vishwani Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 2013

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5203B	Design and Layout of Plants	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**1.** Generate conceptual design for mechatronics / Multi-disciplinary systems based on potential customer **2.** Selection of appropriate microcontrollers, sensors and transducers and devise an instrumentation system for collecting information about processes, control systems. **3.** Selection of appropriate actuators for physical systems. **4.** The course is designed to assist the students in the development of "hands-on" skills with an emphasis on mechatronics/ Multi-disciplinary systems.	**Course Outcomes**	**CO1**	Able to understand the need of mechatronics/Multi-disciplinary systems and integrated product design procedure and role of mechatronics in various engineering fields. — Knowledge
			CO2	Able to understand the various types of modelling, intelligent systems. — Understand
			CO3	Able to understand the appropriate selection of actuators and different control methodology for different types of real life applications. — Apply
			CO4	Able to design and develop innovative solution for industrial applications. — Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	1	1	1	1	1	1	1	1	2	2	1	2	2	1	1
2	CO2	2	2	1	1	1	1	1	1	1	1	2	1	1	2	1
3	CO3	1	1	1	1	1	2	1	2	1	1	2	1	1	1	1
4	CO4	1	1	1	2	2	1	3	1	2	1	1	1	1	1	2
(Average)		1..25	1.25	1.25	1	1.25	1.25	1.25	1.5	1.25	1.5	1.25	1.5	1.25	1.25	1.25

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Introduction to Mechatronics and Intelligent Systems, Definition, scope, and interdisciplinary nature, key components: Mechanical, Electrical, Electronics, and Computer systems for industrial automations. Definition and evolution of intelligent systems, Sensors–computation–decision–actuation loop, Basics of machine learning in control and robotics	**8**	**CO1**
II	System Modeling, Drive controllers for plant automation, Sensors for plant automations, Machine Vision for inspection, Uses of modern technologies, Semi and fully automatic plant layout	**8**	**CO1**
III	Automated Guided Vehicles, types, features, usage. Conveyors: basic functionality requirements, types of Conveyors, application considerations, operational considerations.	**8**	**CO2**
IV	Introduction to facilities planning and design, plant layout, material handling and their interrelationship. Site Location, Warehouse location, Retail location. Case Study: New plant location. Factors affecting plant layout: man, material, machine, movement, waiting, service, building and change, features and considerations of each factor.	**7**	**CO3**
V	Materials Handling: Concept of materials handling, principles of materials handling, factors affecting materials handling, Materials Handling Equipment, Selection of materials handling systems and equipment.	**7**	**CO2, CO3**
VI	Classical types of layouts, Modern Plant Layout, Product layout, Process layout, Fixed-position layouts, Cellular layouts and Hybrid layouts, Product-oriented layout. Production flow-line production, Assembly line balancing. Design of an assembly line, layout heuristics, Assigning tasks in assembly line balancing.	**7**	**CO4**
Total Hours		**45**	

Textbooks:

1. Houshang Karimi, Davood Naghaviha, Hassan Nikkhajoei, (2022) Step-by-Step Design of Large-Scale Photovoltaic Power Plants, 1119736560, 9781119736561, Wiley
2. Houtan Jebelli, Mahmoud Habibnezhad, Shayan Shayesteh, Somayeh Asadi, Sang Hyun Lee, (2022), Automation and Robotics in the Architecture, Engineering, and Construction Industry, 3030771628, 9783030771621, Springer
3. Jutta Geldermann, (2010) Integrated Process Design for the Inter-Company Plant Layout Planning of Dynamic Mass Flow Networks, 3866441266, 9783866441262, KIT Scientific Publishing

Reference Books:

1. J. Fahed-Sreih, (2018). Human Resource Planning for the 21st Century, London, Intech Open
2. B. Badhai, (2019). Entrepreneurship Development, B. K. Publications Private Limited.
3. Wasiyoddin R. Mujawar, (2019). Psychology of Social Work Practice, Oxford publication.
4. Nicholas Odrey, Mitchell Weiss, Mikell Groover, Roger Nage, Ashish Dutta, (2017). Industrial Robotics -Technology ,Programming and Applications, SIE Publication

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CURRICULUM

Programme	M. Tech in Microelectronics & Intelligent System	**Academic Year of Regulation**	**2025-26**
Department	Electronics & Communication Engineering	**Semester**	**II**

Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5203C	VLSI Technology & Fabrication	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. Understand the Fabrication Process of IC Technology
2. Understand the concept of conversion of a single crystal of silicon into an IC requires.
3. Exposer to different fabrication steps such as epitaxy, oxidation, chemical vapor deposition, metallization.
4. Understand the concepts of ion implantation, etching and lithography.

Course Outcomes		
CO1	Understand the basic steps of MOS transistor fabrication.	Knowledge
CO2	Learn the basics theory of Crystal Growth and Wafer Preparation.	Understand
CO3	Students understand the concepts of Epitaxy, Diffusion, Oxidation, Lithography and Etching.	Apply
CO4	Understands the process of film deposition and metallization in Chip manufacturing	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	3	1	0	0	0	0	0	0	0	0	2	2	2
2	CO2	2	2	3	1	0	0	0	0	0	0	0	0	2	2	2
3	CO3	3	2	3	1	0	0	0	0	0	0	0	0	2	2	2
4	CO4	3	2	3	1	0	0	0	0	0	0	0	0	2	2	2
(Average)		2.75	2	3	1	0	0	0	0	0	0	0	0	2	2	2

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, NMOS IC Technology, CMOS IC Technology, MOS Memory IC Technology, IC Fabrication.	**8**	**CO1**
II	Crystal Growth and Wafer Preparation: Introduction, Electronic grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Processing Considerations	**8**	**CO2**
III	Epitacy: Introduction, Vapor Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation. Oxidation: Introduction, Growth Mechanism and Kinematics, Thin Oxides, Oxidation Techniques and Systems, Oxidation of Polysilicon	**8**	**CO3**
IV	Lithography: Introduction, Optical Lithography, Electron Lithography, Ion Lithography, Plasma properties, Feature size control and Anisotropic Etch Mechanism, Reactive Plasma Etching Techniques and Equipment, Specific Etch Process.	**8**	**CO3**
V	Dielectric and Polysilicon Film Deposition: Introduction, Deposition Process, Polysilicon, Silicon Dioxide, Automatic Diffusion Mechanism, Measurement Techniques, Range Theory, Metalization, Metalization Applications, Metalization Choices, Patterning, Metalization Problems.	**8**	**CO4**
Total Hours			

Textbooks:

1. S.M. Sze, VLSI Technology, McGraw Hill Companies Inc. 2nd Edition, 2017
2. C.Y. Chang and S.M. Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996

Reference Books:

1. S. A. Campbell, The Science and Engineering of Microelectronic Fabrication, 2nd Edition, Oxford University Press, 2001
2. J. D. Plummer, M. Deal, P. Griffin, Silicon VLSI Technology, Pearson Education, 1st Edition, 2000

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		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5204A	CAD for VLSI	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives

1. To introduce mathematical and algorithmic foundations for computer-aided design in VLSI.
2. To develop understanding of graph theory, matrix theory, and their applications in VLSI CAD.
3. To learn algorithms used for VLSI physical design automation and circuit simulation.
4. To explore advanced CAD techniques for FPGA/CPLD design, fault tolerance, and testing.

Course Outcomes

CO1	Explain matrix and graph theoretic concepts relevant to VLSI CAD	Knowledge
CO2	Apply data structures and algorithms to solve computational design problems.	Understand
CO3	Analyze and implement algorithms for physical design, synthesis, and simulation.	Apply
CO4	Evaluate CAD methodologies for FPGA/CPLD design, fault tolerance, and testing	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	1	1	2	0	0	0	0	0	0	0	3	2	1
2	CO2	2	3	2	2	3	0	0	0	0	0	0	0	3	3	2
3	CO3	2	3	3	3	3	1	0	0	0	0	0	0	3	3	3
4	CO4	1	2	3	3	2	1	0	0	0	0	0	0	3	3	3
(Average)		2	2.5	2.25	2.25	2.5	0.5	0	0	0	0	0	0	3	2.75	2.75

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	***Matrices*:** Linear dependence of vectors, Solution of linear equations, Bases of vector spaces, orthogonality, Complementary orthogonal spaces and solution spaces of linear equations. ***Graphs*:** Representation of graphs using matrices, Paths, Connectedness, Circuits, Cutsets, Trees, Fundamentals circuit and cutset matrices, Voltage and current spaces of a directed graph and their complementary orthogonality.	**10**	**CO1**
II	***Algorithms and data structures*:** Efficient representation of graphs, Elementary graph algorithms involving BFS and DFS trees, Such as finding connected and 2-connected components of a graph, The minimum spanning tree, Shortest path between a pair of vertices in a graph.	**10**	**CO2**
III	Algorithms for VLSI physical design, Synthesis, Circuit simulation and digital design automation.	**10**	**CO3**
IV	Algorithms for design automation using FPGA/CPLD, Fault tolerant systems, VLSI testing.	**10**	**CO4**
	Total Hours	**40**	

Textbooks:

1. K. Hoffman and R.A. Kunze, "Linear Algebra", Prentice Hall, 1986.
2. N. Balabanian and T.A. Bickart, "Linear Network Theory; Analysis, Properties, Design and Synthesis", Matrix Publishers, Inc., 1981.
3. T. H.Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms", MIT press and McGraw-Hill, 1990.

Reference Books:

1. N. Shervani, "Algorithms for VLSI Physical Design Automation", 3/e, Kluwer Academic Publishers, 1998
2. W. J. McCalla, "Fundamentals of Computer-Aided Circuit Simulation", Kluwer Academic Publishers, 1987
3. G. De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw Hill, 2003.

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Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**INT**	**MID**	**END**	**Total**	**Bloom's taxonomy**
EC-5204B	Memory Subsystem	**3**	**0**	**0**	**3**	**20**	**30**	**50**	**100**	

Course Objectives	**Course Outcomes**		
1. Understand memory hierarchy and design principles. **2.** Analyze cache architectures and performance. **3.** Study DRAM and NVM technologies and system integration. **4.** Evaluate and design optimized low-power memory subsystems.	**CO1**	Explain memory hierarchy concepts and performance metrics.	Knowledge
	CO2	Analyze cache architectures and replacement policies.	Understand
	CO3	Evaluate DRAM/NVM systems in terms of power and scalability.	Apply
	CO4	Design optimized memory subsystems and simulate performance.	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	0	0	0	0	0	0	0	0	0	0	3	2	0
2	CO2	3	3	2	0	0	0	0	0	0	0	0	0	3	3	0
3	CO3	3	3	3	2	0	0	0	0	0	0	0	0	3	3	2
4	CO4	3	3	3	3	2	0	0	0	0	0	0	0	3	3	2
(Average)		3	2.75	2	1.25	0.5	0	0	0	0	0	0	0	3	2.75	1

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Overview of computer memory hierarchy, design goals, metrics (latency, bandwidth, hit rate)	**6**	**CO1**
II	Cache organization: direct-mapped, set-associative, fully associative; write/read policies Cache coherence and consistency, multi-core shared caches, prefetching, and replacement	**12**	**CO2**
III	Main memory architecture: a) SRAM, b) DRAM cell, timing, refresh, and controller design, c) BCAM / TCAM Non-volatile memories (PCM, MRAM, ReRAM, 3D XPoint) — principles and integration	**12**	**CO3**
IV	Power, energy, and reliability issues in memory subsystem Memory scheduling, bandwidth optimization, and QoS	**6**	**CO3, CO4**
V	Design case studies: CPU/GPU memory systems, SoC integration Emerging trends: 3D-stacked memory, HBM, CXL, and persistent memory	**6**	**CO4**
Total Hours			

Textbooks:

1. John L. Hennessy & David A. Patterson, *Computer Architecture: A Quantitative Approach*, 6th Ed., Morgan Kaufmann, 2019.
2. Bruce Jacob, Spencer Ng, and David Wang, *Memory Systems: Cache, DRAM, Disk*, Morgan Kaufmann, 2010.

Reference Books:

1. Y. Solihin, *Fundamentals of Parallel Multicore Architecture*, CRC Press, 2015.
2. W. Wolf, *Modern VLSI Design: System-on-Chip Design*, Pearson, 2014.

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Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**Attend.**	**Exam**	**Viva**	**Total**	**Bloom's taxonomy**
EC-5202	VLSI Laboratory II	**0**	**0**	**4**	**2**	**20**	**50**	**30**	**100**	

Course Objectives

1. To provide hands-on experience with MOSFET device characterization and analog circuit building blocks.
2. To develop practical understanding of standard cell design for amplifiers and current mirrors.
3. To design, simulate, and layout analog building blocks like op-amps, oscillators, and PLLs.
4. To correlate theoretical circuit analysis with simulation and layout outcomes.

Course Outcomes

CO1	Demonstrate understanding of NMOS/PMOS device characteristics and current equations.	Knowledge
CO2	Design and simulate analog building blocks such as amplifiers and current mirrors.	Understand
CO3	Develop and layout complex analog circuits such as op-amps and oscillators.	Apply
CO4	Analyze and evaluate performance metrics (gain, frequency, phase margin, power) of analog VLSI circuits.	Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1	CO1	3	2	2	1	2	0	0	0	0	0	0	0	3	2	0
2	CO2	3	3	3	2	2	0	0	0	0	0	0	0	3	3	2
3	CO3	3	3	3	3	2	0	0	0	0	0	0	0	3	3	2
4	CO4	3	3	3	3	3	0	0	0	0	0	0	0	3	3	2
(Average)		3	2.75	2.75	2.25	2.25	0	0	0	0	0	0	0	3	2.75	1.5

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	Characterization of NMOS & PMOS Transistor (both DC and AC) and Analysis of current equation.	**40**	**CO1, CO2, CO3, CO4**
II	Characterization of NMOS & PMOS based MOSCAP.		
III	Standard Cell design of a Common Source / Common Gate / Common Drain Amplifier		
IV	Standard Cell design of a Single stage Cascode Amplifier		
V	Standard Cell design of a Current Mirror along with Differential Pair		
VI	Design of a single and two-stage Op-Amp		
VII	Design and layout of a ring oscillator and VCO		
VIII	Design and Analysis of an ideal PLL circuit.		
Total Hours		**40**	

Textbooks:

1. Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 3e, Tata Mc Graw-Hill, 2007.
2. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill Education, 2e, 2017.

Reference Books:

1. A. S. Sedra and K. C. Smith, Microelectronic Circuits, Oxford University Press, 7e, 2014
2. P. R. Gray, R. G. Meyer, P. J. Hurst and S. H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley International, 4e, 2005.
3. Michael Jacob, Applications and Design with Analog Integrated Circuits, Prentice Hall of India, 2e, 1996.

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Course Code	**Course Name**	**Credit Structure**					**Marks Distribution**			
		L	**T**	**P**	**C**	**Attend.**	**Exam**	**Viva**	**Total**	**Bloom's taxonomy**
EC-5203	Embedded Systems & IoT Laboratory II	**0**	**0**	**4**	**2**	**20**	**50**	**30**	**100**	

Course Objectives	**1.** To impart practical knowledge of embedded system design, simulation, and interfacing using modern tools. **2.** To develop skills for real-time control and IoT-based embedded applications. **3.** To use ARM and microcontroller platforms for hardware/software co-design. **4.** To implement and evaluate embedded and IoT projects with sensors, actuators, and communication interfaces.	**Course Outcomes**	**CO1**	Explain the architecture and working principles of embedded and IoT systems. — Knowledge
			CO2	Develop and debug embedded applications using ARM-based platforms and simulation tools. — Understand
			CO3	Integrate hardware and software modules to realize embedded automation and control systems. — Apply
			CO4	Analyze embedded system performance and security aspects in IoT contexts. — Analyze

No.	**COs**	**Mapping with Program Outcomes (POs)**												**Mapping with PSOs**		
		PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
1.	CO1	3	2	2	1	2	0	0	0	0	0	0	0	3	2	0
2.	CO2	3	3	3	2	2	0	0	0	0	0	0	0	3	3	2
3.	CO3	3	3	3	3	2	0	0	0	0	0	0	0	3	3	2
4.	CO4	3	3	3	3	3	0	0	0	0	0	0	0	3	3	2
(Average)		3	2.75	2.75	2.25	2.25	0	0	0	0	0	0	0	3	2.75	1.5

SYLLABUS

No.	**Content**	**Hours**	**COs**
I	To study distributed embedded system using Proteus design suit.	**4**	**CO1, CO2, CO3, CO4**
II	Robot multiple link joint controller for industrial automation.	**4**	
III	ARM based embedded system design using μ Keil simulator and implementation using ARM	**4**	
IV	Demonstrate ARM Cortex-M Programming using μ Keil and debugging using Unilink LED pattern design using input/output ports.	**4**	
V	To study timing analysis using logic analyzer for automatic material handling system.	**4**	
VI	To study the embedded security for embedded system.	**4**	
VII	To study embedded system development techniques using Matlab.	**4**	
VIII	To study embedded system development techniques using Labview.	**4**	
	Total Hours	**32**	

Textbooks:

1. James K. Peckol, Anikt A. Bhurane, Dushyant K. Sing, Lachit Dutta, Sahadev Roy, Trailokya Nath Sasamal "Embedded Systems A Contemporary Design Tool", Wiley , 378-93-5746-396-6, (2024)
2. M A Mazidi, J G Mazidi, R D McKinlay, The 8051 Microcontroller and Embedded Systems Using Assemble and C, Pearson/Prentice Hall, 2nd Ed
3. Lyla B Das; Embedded Systems and Integrated Approach, Pearson, India, 2013, first edition,
4. Rajkamal, Microcontrollers, Archi, Progr, interfacing and Sys design, Pearson, India, 2nd ed, 2012

Reference Books:

1. Kenneth Ayala, The 8051 Microcontroller, Cengage learning, India, 2004 3rd Ed
2. K M Bhurchandi, A K Ray, Advanced microprocessors and Peripherals, McGraw Hill Education India, 2012, 3rd ed Top
3. K V Shibu, Introduction to Embedded Systems, Tata McGraw Hill Education, India, 2009